DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

M.E. VLSI DESIGN

Regulation 2023

CHOICE BASED CREDIT SYSTEM

(I - IV SEMESTERS CURRICULUM & SYLLABUS)

Sri Eshwar College of Engineering

(An Autonomous Institution)

(Approved by AICTE, Affiliated to Anna University, Chennai)

Kondampatti (Post), Kinathukadavu,

Coimbatore- 641202.

M.E. VLSI Design

Regulation 2023

Semester I

Sl. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
THEORY								
1	P23MA201	Mathematics for VLSI Engineers	FC	4	3	1	0	4
2	P23VL401	Semiconductor Devices and Modeling	PC	3	3	0	0	3
3	P23VL402	CMOS Digital VLSI Design	PC	3	3	0	0	3
4	P23VL403	FPGA Based System Design	PC	3	3	0	0	3
5	P23VL404	Analog IC Design	PC	3	3	0	0	3
6	P23VL5XX	Program Elective I	PE	3	3	0	0	3
PRACTICALS								
7	P23VL451	Front-End Simulation and FPGA Lab	PC	4	0	0	4	2
8	P23VL452	Analog IC Design Lab	PC	4	0	0	4	2
9	P23AC9XX	Audit Course	AC	2	2	0	0	NC
		TOTAL		**29**	**20**	**1**	**8**	**23**

Semester II

Sl. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
THEORY								
1	P23VL405	ASIC Design	PC	3	3	0	0	3
2	P23VL406	Design for Testability	PC	3	3	0	0	3
3	P23VL407	Low Power IC Design	PC	3	3	0	0	3
4	P23VL5XX	Program Elective II	PE	3	3	0	0	3
5	P23VL5XX	Program Elective III	PE	3	3	0	0	3
6	P23VL5XX	Program Elective IV	PE	3	3	0	0	3
PRACTICALS								
7	P23VL453	ASIC Design Lab	PC	4	0	0	4	2
8	P23VL454	Design for Testability Lab	PC	4	0	0	4	2
		Value Added Course	PC	2	-	-	-	-
		TOTAL		**28**	**18**	**0**	**8**	**22**

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Semester III

Sl. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
THEORY								
1	P23VL5XX	Program Elective V	PE	3	3	0	0	3
2	P23VL5XX	Program Elective VI	PE	3	3	0	0	3
3	P23OXXXX	Open Elective	OE	3	3	0	0	3
PRACTICALS								
3	P23VL601	Project Work Phase I	PW	16	0	0	16	8
		TOTAL		**25**	**9**	**0**	**16**	**17**

Semester IV

Sl. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
PRACTICALS								
1	P23VL602	Project Work Phase II	PW	32	0	0	32	16
		TOTAL		**32**	**0**	**0**	**32**	**16**

TOTAL NO. OF CREDITS: 78

SUMMARY

Sl.No.	Course Category	Credits per semester				Credits	Credit%
		I	II	III	IV		
1	**FC**	4	-	-	-	04	
2	**PC**	16	13			29	
3	**PE**	3	9	6	-	18	
4	**OE**	-	-	3	-	03	
5	**PW**	-	-	8	16	24	
6	**MC**	-	-	-	-	-	
7	**AC**	-	-	-	-	-	
Total						**78**	

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FOUNDATION COURSE (FC)

Sl. No.	Course Code	Subject	Course Category	L	T	P	C
1	P23MA201	Mathematics for VLSI Engineers	FC	3	1	0	4

PROGRAM CORE (PC)

Sl. No.	Course Code	Subject	Course Category	L	T	P	C
1	P23VL401	Semiconductor Devices and Modeling	PC	3	0	0	3
2	P23VL402	CMOS Digital VLSI Design	PC	3	0	0	3
3	P23VL403	FPGA Based System Design	PC	3	0	0	3
4	P23VL404	Analog IC Design	PC	3	0	0	3
5	P23VL405	ASIC Design	PC	3	0	0	3
6	P23VL406	Design for Testability	PC	3	0	0	3
7	P23VL407	Low Power IC Design	PC	3	0	0	3

PROGRAM ELECTIVES (PE)

Sl. No.	Course Code	Subject	Course Category	L	T	P	C
SEMESTER I–ELECTIVE I							
1	P23VL501	CAD for VLSI Circuits	PE	3	0	0	3
2	P23VL502	Advanced Digital System Design	PE	3	0	0	3
3	P23VL503	VLSI for IoT systems	PE	3	0	0	3
4	P23VL504	Electromagnetic Interference and Compatibility	PE	3	0	0	3
SEMESTER II–ELECTIVE II							
5	P23VL506	Hardware Design and Verification Languages	PE	3	0	0	3
6	P23VL505	VLSI Signal Processing	PE	3	0	0	3
7	P23VL507	DSP Processor Architecture and Programming	PE	3	0	0	3
8	P23VL508	Hardware Software Co-Design for FPGA	PE	3	0	0	3
SEMESTER II–ELECTIVE III							
9	P23VL509	Scripting Languages for VLSI	PE	3	0	0	3
10	P23VL510	VLSI for Wireless Communication	PE	3	0	0	3
11	P23VL511	Soft Computing and Optimization Techniques	PE	3	0	0	3
12	P23VL512	Reconfigurable Architectures	PE	3	0	0	3
SEMESTER II–ELECTIVE IV							
13	P23VL513	Hardware Architectures for Artificial Intelligence and Machine Learning	PE	3	0	0	3
14	P23VL514	System-on-Chip Design	PE	3	0	0	3
15	P23VL515	Networks on Chip	PE	3	0	0	3
16	P23VL516	Design and Analysis of Computer Algorithms	PE	3	0	0	3
SEMESTER III–ELECTIVE V							
17	P23VL517	Semiconductor Memory Design	PE	3	0	0	3
18	P23VL518	Signal Integrity for High-Speed Design	PE	3	0	0	3
19	P23VL519	Nanoscale Devices	PE	3	0	0	3
20	P23VL520	MEMS and NEMS	PE	3	0	0	3
SEMESTER III–ELECTIVE VI							
21	P23VL521	RF IC Design	PE	3	0	0	3
22	P23VL522	Hardware Security	PE	3	0	0	3
23	P23VL523	Electronic Packaging Technologies	PE	3	0	0	3
24	P23VL524	Advanced Computer Architecture and Parallel Processing	PE	3	0	0	3

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OPEN ELECTIVES (OE)

Sl. No	Course Code	Subject	Course Category	L	T	P	C
1	P23OE501	Business Analytics	OE	3	0	0	3
2	P23OE502	Industrial Safety	OE	3	0	0	3
3	P23OE503	Operations Research	OE	3	0	0	3
4	P23OE507	Artificial Intelligence	OE	3	0	0	3
5	P23OE508	Machine Learning	OE	3	0	0	3

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SEMESTER – I

Sl. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
THEORY								
1	P23MA201	Mathematics for VLSI Engineers	FC	4	3	1	0	4
2	P23VL401	Semiconductor Devices and Modeling	PC	3	3	0	0	3
3	P23VL402	CMOS Digital VLSI Design	PC	3	3	0	0	3
4	P23VL403	FPGA Based System Design	PC	3	3	0	0	3
5	P23VL404	Analog IC Design	PC	3	3	0	0	3
6	P23VL5XX	Program Elective I	PE	3	3	0	0	3
PRACTICALS								
7	P23VL451	Front-End Simulation and FPGA Lab	PC	4	0	0	4	2
8	P23VL452	Analog IC Design Lab	PC	4	0	0	4	2
9	P23AC9XX	Audit Course I	AC	2	2	0	0	NC
TOTAL				**29**	**20**	**1**	**8**	**23**

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P23MA201	MATHEMATICS FOR VLSI ENGINEERS	L	T	P	C
		3	1	0	4

1. Course Description

This course covers essential graph theory concepts including terminology, algorithms, and connectivity, alongside linear and nonlinear programming techniques such as simplex method and KKT conditions. Additionally, it explores simulation modeling including Monte Carlo simulation and discrete event simulation elements, providing students with a comprehensive understanding of mathematical modeling and optimization methods.

2. Course Objectives:

1. To introduce graphs as mathematical models to solve connectivity-related problems.
2. To introduce fundamental graph algorithms
3. To provide knowledge on non-linear programming
4. To understand the applications of simulation modelling in engineering problems.
5. To solve real-world problems using these mathematical tools and algorithms.

3. Syllabus

Unit-I: Graphs

Graphs and graph models – Graph terminology and special types of graphs – Matrix representation of graphs and graph isomorphism – Connectivity – Euler and Hamilton paths.

Unit-II: Graph Algorithm

Graph Algorithms – Directed graphs – Some basic algorithms – Shortest path algorithms – Depth – First search on a graph – Theoretic algorithms – Performance of graph theoretic algorithms – Graph theoretic computer languages.

Unit-III: Linear Programming

Formulation – Graphical solution – Simplex method – Two-phase method – Transportation and Assignment Models.

Unit-IV: Non-Linear Programming

Constrained Problems – Equality constraints – Lagrangean Method – Inequality constraints – Karush – Kuhn-Tucker (KKT) conditions – Quadratic Programming.

Unit-V: Simulation Modelling

Monte Carlo Simulation – Types of Simulation – Elements of Discrete Event Simulation – Generation of Random Numbers – Applications to Queuing Systems.

References:

Reference Books

1. Taha H.A, "Operation Research: An Introduction", Ninth Edition, Pearson Education, New Delhi, 2010.
2. Gupta P. K, and Hira D.S., "Operation Research", Revise Edition, S. Chand and Company Ltd., 2012.
3. Sharma J.K., "Operation Research", 3rd Edition, Macmillan Publishers India Ltd., 2009.
4. Douglas B. West, "Introduction to Graph Theory", Pearson Education, New Delhi, 2015.
5. Balakrishna R., Ranganathan. K., "A text book of Graph Theory", Springer Science and Business Media, New Delhi, 2012.

Journals:

1. https://www.sciencedirect.com/journal/integration
2. https://jics.org.br/ojs/index.php/JICS

Video Reference:

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1. https://www.youtube.com/watch?v=09_LlHjoEiY
2. https://hal.science/hal-01901499/document

NPTEL Courses:

1. https://www.coursera.org/courses?query=graph%20theory
2. https://www.udemy.com/course/graph-theory

4. Course Outcomes

CO. No.	Course Outcome
P23MA201.1	Concepts of graph theory, knowledge representation using graph theory, propositions, and applications
P23MA201.2	Apply different techniques in graph algorithms to solve complex problems
P23MA201.3	Test the nature of linear programming and analyze the consistency of solutions to linear programming problems
P23MA201.4	Apply the principles of optimality, formulation, and computational procedure of non-linear programming
P23MA201.5	Examine the basic concepts using Monte Carlo Simulation and acquire skills in Queuing systems applications

P23VL401	SEMICONDUCTOR DEVICES AND MODELING	L	T	P	C
		3	0	0	3

1. Course Description

This course provides a comprehensive understanding of the principles and applications of semiconductor devices and their modeling. It is designed to equip students with the knowledge required to analyze, design, and model semiconductor devices used in modern electronics.

2. Course Objectives:

1. To review the basic MOSFET structures and characteristics
2. To impart knowledge on MOS models in simulation
3. To introduce FINFETs and other multi-gate transistors.
4. To provide practical knowledge on design tools for device modelling.
5. To understand MOSFET models, behaviour under different operational conditions, simulation through SPICE, and the challenges of scaling and fabrication.

3. Syllabus

Unit-I: MOSFET Model

Introduction to MOSFET - Output and Transfer Characteristics - MOS Capacitor - Long, Short Channel MOSFETs–Non-Ideal Effects - MOSFET Scaling - Threshold Voltage - Small Signal Model - Large Signal Model - MOSFET Parasitic Capacitances.

Unit-II: SPICE Model For MOSFET

SPICE Models for Semiconductor Devices - MOSFET Level1, Level2, and Level 3 Models - BSIM Model - Model Parameters - Models for Semiconductor Contacts and Hetero Junctions - Charge Control Models - Second Order Effects - Velocity Saturation and Universal Models

Unit-III: Compact Models

FINFETs - SOI MOSFETs - Single Gate to Multi Gate Transformation - Multigate MOSFET Technology - Physics of Multigate MOS - Mobility in Multi-gate MOSFET.

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Unit-IV: Fabrication Requirements and Challenges
Radiation Effects in Single Gate and Multi-Gate FETs - Single Event Effects – Multi-Gate MOSFET Circuit Design - Double Gate MOSFET - Drain Current Model - Fabrication Requirements and Challenges - SoC Design
Unit-V: Scaling and Short Channel Effects
Effect of scaling - Channel length modulation - Punch-through - Hot carrier degradation - MOSFET breakdown - Drain-induced barrier lowering.
References:
Reference Books 1. D.A.Neamen, Semiconductor Physics and Devices: Basic Principle, Third Edition, McGraw – Hill International, 2003 2. J.P. Colinge and C. A. Colinge, Physics of Semiconductor Devices, Kluwer Academic Publishers, US, 2017. 3. Y.Taur and T.H. Ning, Fundamentals of Modern VLSI Devices, Second Edition, Cambridge University Press, 2009 4. Ben G. Streetman and S. Banerjee, Solid State Electronic Devices, Pearson Education, U.S, Seventh Edition, 2014 **Journals:** 1. https://iopscience.iop.org/journal/1674-4926 **Video Reference:** 1. https://www.digimat.in/nptel/courses/video/117106033/L01.html **NPTEL Courses:** 1. https://onlinecourses.nptel.ac.in/noc23_ee35/preview 2. https://www.coursera.org/specializations/semiconductor-devices

4. Course Outcomes

CO. No.	Course Outcome
P23VL401.1	Understand the MOSFET structure evolution, types, and working principle.
P23VL401.2	Apply the knowledge to model devices using simulation.
P23VL401.3	Analyze the device behavior and characteristics of multigate transistors.
P23VL401.4	Investigate the radiation issues and learn fabrication challenges.
P23VL401.5	Understand device scaling and short-channel effects.

P23VL402	CMOS DIGITAL VLSI DESIGN	L	T	P	C
		3	0	0	3

1. Course Description
This course offers an in-depth exploration of CMOS (Complementary Metal-Oxide-Semiconductor) technology and its application in the design and analysis of digital Very Large Scale Integration (VLSI) circuits. It aims to provide students with the theoretical background and practical skills necessary to design, simulate, and implement CMOS digital circuits.
2. Course Objectives:
1. To introduce the transistor-level design of all digital building blocks common to all CMOS microprocessors, network processors, digital backend of all wireless systems, etc

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2. To introduce the principles and design methodology in terms of the dominant circuit choices, constraints, and performance measures
3. To learn all important issues related to size, speed, and power consumption
4. To introduce to different combinational logic design techniques, including static and dynamic CMOS design styles, complex gates, and interconnect delays, with a focus on optimizing performance.
5. To introduce the architecture and design of memory systems, including ROM, RAM, dynamic memory, SRAM, and sense amplifiers, with an emphasis on trade-offs between speed, area, and power.

3. Syllabus

Unit-I: MOS Transistor Principles and CMOS Inverter

MOSFET Transistor Characteristic under Static and Dynamic Conditions, MOS Transistor Secondary Effects, Technology Scaling - Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay parameters, stick diagram and layout diagrams.

Unit-II: Combinational Logic Circuits

Static CMOS design, different styles of logic circuits, logical effort of complex gates, static and dynamic properties of complex gates, interconnect delay, and dynamic logic gates.

Unit-III: Sequential Logic Circuits

Static latches and registers, dynamic latches and registers, timing issues, pipelines, clocking strategies, and non-bistable sequential circuits.

Unit-IV: Arithmetic Building Blocks

Data path circuits, Architectures for Adders, Accumulators, Multipliers, Speed and Area Tradeoffs.

Unit-V: Memory Architectures

Memories, ROM cells, Read-Write Memories (RAM), dynamic memory design, 6 Transistor SRAM cell, sense amplifiers.

References:

Reference Books

1. M J Smith, "Application Specific Integrated Circuits", Addison Wesley, 2014.
2. Neil H.E. Weste, David Harris, Ayan Banerjee "CMOS VLSI Design", Third Edition, Pearson, 2006
3. Jacob Baker "CMOS: Circuit Design, Layout, and Simulation, 3rd Edition", Wiley Press 2010.
4. Jan Rabaey, AnanthaChandrakasan, B Nikolic, "Digital Integrated Circuits: A Design Perspective". Second Edition, Prentice Hall of India, 2003

Journals:

1. https://ieeexplore.ieee.org/document/663545

Video Reference:

1. https://www.youtube.com/watch?v=oL8SKNxEaHs&list=PLLy_2iUCG87Bdulp9brz9AcvW_TnFCUmM
2. https://www.youtube.com/watch?v=oenQPhwaKnM

NPTEL Courses:

1. https://www.udemy.com/course/cmos-digital-vlsi-design-lab/
2. https://onlinecourses.nptel.ac.in/noc21_ee09/preview

4. Course Outcomes

CO. No.	Course Outcome
P23VL402.1	Understand the performance of CMOS Inverter circuits on the basis of their operation and working

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P23VL402.2	Analyze the static CMOS Combinational logic circuits
P23VL402.3	Design sequential logic at the transistor level and compare the tradeoffs
P23VL402.4	Understand the design methodology of arithmetic building blocks
P23VL402.5	Design functional units including ROM and SRAM

P23VL403	FPGA BASED SYSTEM DESIGN	L	T	P	C
		3	0	0	3

1. Course Description

This course focuses on the design, implementation, and testing of digital systems using Field-Programmable Gate Arrays (FPGAs). It covers the theoretical concepts of digital design and provides practical experience in hardware description languages (HDLs) and FPGA development tools. Students will learn to design complex digital systems, synthesize them onto FPGAs, and verify their functionality.

2. Course Objectives:

1. To design simple digital systems using PLDs
2. To analyse the architecture of FPGA
3. To analyse the design considerations of FPGA
4. To Learn Placement and Routing Techniques
5. To understand Commercial FPGA and Memory Architectures

3. Syllabus

Unit-I: Basics of Digital System Design

Digital system design options and tradeoffs, Design methodology and technology overview, High Level System Architecture and Specification: Behavioral modeling and simulation, Hardware description languages (emphasis on Verilog), combinational and sequential design, state machine design, synthesis issues, test benches.

Unit-II: Programmable Logic Devices

ROM, PLA, PAL, CPLD, FPGA Features, Limitations, Architectures and Programming. Implementation of MSI circuits using Programmable logic Devices.

Unit-III: FPGA Architecture

FPGA Architectural options, granularity of function and wiring resources, coarse V/s fine grained, vendor specific issues (emphasis on Xilinx and Altera), Logic block architecture: FPGA logic cells, timing models, power dissipation I/O block architecture: Input and Output cell characteristics, clock input, Timing, Power dissipation.

Unit-IV: Placement and Routing

Programmable interconnect - Partitioning and Placement, Routing resources, delays; Applications - Embedded system design using FPGAs, DSP using FPGAs.

Unit-V: Commercial FPGAs

Memories, ROM cells, Read-Write Memories (RAM), dynamic memory design, 6 Transistor SRAM cell, sense amplifiers.

References:

Reference Books

1. FPGA-Based System Design Wayne Wolf, Verlag: Prentice Hall, 2004
2. Modern VLSI Design: System-on-Chip Design (3rd Edition) Wayne Wolf, Verlag, 2002

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3. Field Programmable Gate Array Technology - S. Trimberger, Edr, 1994, Kluwer Academic, 2012
4. Digital Design Using Field Programmable Gate Array, P.K. Chan & S. Mourad, 1994, Prentice Hall

Journals:

1. https://ieeexplore.ieee.org/document/9391086

Video Reference:

1. https://www.youtube.com/watch?v=oL8SKNxEaHs&list=PLLy_2iUCG87Bdulp9brz9AcvW_TnFCUmM
2. https://www.youtube.com/watch?v=oenQPhwaKnM

NPTEL Courses:

1. https://www.udemy.com/course/cmos-digital-vlsi-design-lab/
2. https://onlinecourses.nptel.ac.in/noc21_ee09/preview

4. Course Outcomes

CO. No.	Course Outcome
P23VL403.1	Design simple digital systems with programmable logic devices
P23VL403.2	Analyze the architecture of FPGA
P23VL403.3	Analyze the design considerations of FPGA
P23VL403.4	Understand the placement and routing in FPGAs
P23VL403.5	Design simple combinational and sequential circuits using FPGA

P23VL404	ANALOG IC DESIGN	L	T	P	C
		3	0	0	3

1. Course Description

This course offers an in-depth study of the principles, techniques, and tools used in the design and analysis of analog integrated circuits (ICs). It covers the theoretical foundations of analog electronics and provides practical experience in designing and simulating analog ICs. Students will learn to design fundamental analog building blocks, understand their limitations, and optimize their performance for various applications.

2. Course Objectives:

1. To study single-stage and two-stage amplifiers.
2. To understand the frequency response of single-stage and two-stage amplifiers.
3. To understand the concepts of feedback and single-stage OPAMPS.
4. To study current mirrors, reference circuits, and OPAMP Characteristics.
5. To analyze High Frequency and Noise Characteristics

3. Syllabus

Unit-I: Single-Stage Amplifiers

Basic MOS physics and equivalent circuits and models, CS, CG and Source Follower, differential amplifier with active load, Cascode and Folded Cascode configurations with active load, design of Differential and Cascode Amplifiers – to meet specified SR, noise, gain, BW, ICMR and power dissipation, voltage swing, high gain amplifier structures.

Unit-II: High Frequency and Noise Characteristics of Amplifiers

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Miller effect, association of poles with nodes, frequency response of CS, CG and Source Follower, Cascode and Differential Amplifier stages, statistical characteristics of noise, noise in Single Stage amplifiers, noise in Differential Amplifiers.
Unit-III: Feedback and Single Stage Operational Amplifiers
Properties and types of negative feedback circuits, effect of loading in feedback networks, operational amplifier performance parameters, single stage Op Amps, two-stage Op Amps, input range limitations, gain boosting, slew rate, power supply rejection, noise in Op Amps.
Unit-IV: Stability And Frequency Compensation of Two Stage Amplifier
Analysis Of Two Stage Op Amp – Two Stage Op Amp Single Stage CMOS CS as Second Stage and Using Cascode Second Stage, Multiple Systems, Phase Margin, Frequency Compensation, And Compensation of Two Stage Op Amps, Slewing In Two Stage Op Amps, Other Compensation Techniques.
Unit-V: Bandgap References
Current sinks and sources, current mirrors, Wilson current source, Widlar current source, cascode current source, design of high swing cascode sink, current amplifiers, supply independent biasing, temperature independent references, PTAT and CTAT current generation, constant-gm biasing.
References:
Reference Books 1. BehzadRazavi, "Design of Analog CMOS Integrated Circuits", Tata Mcgraw Hill, 2001. 2. Willey M.C. Sansen, "Analog Design Essentials", Springer, 2006. 3. Grebene, "Bipolar and MOS Analog Integrated Circuit Design", John Wiley & Sons, 2003. 4. Phillip E.Allen, Douglas R .Holberg, "CMOS Analog Circuit Design", Oxford University Press, 2nd Edition, 2002. 5. Recorded Lecture Available at http://www.ee.iitm.ac.in/vlsi/courses/ee5320_2021/start, 6. Jacob Baker "CMOS: Circuit Design, Layout, And Simulation, Wiley lEEE Press, 3/e, 2010. **Journals:** 1. https://link.springer.com/journal/10470 **Video Reference:** 1. https://onlinecourses.nptel.ac.in/noc21_ee51/preview 2. https://archive.nptel.ac.in/courses/117/106/117106030/ **NPTEL Courses:** 1. https://nptel.ac.in/courses/108106105 2. https://www.udemy.com/topic/analog-circuits/

4. Course Outcomes

CO. No.	Course Outcome
P23VL404.1	Analyze single-stage amplifiers with MOS loads.
P23VL404.2	Analyze the concepts of frequency response and noise characteristics of differential amplifiers.
P23VL404.3	Design and model different active devices with OPAMPs.
P23VL404.4	Interpret the multi-pole systems and frequency compensations techniques.
P23VL404.5	Design current sources at the CMOS transistor level.

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P23VL451	FRONT-END SIMULATION AND FPGA LAB	L	T	P	C
		0	0	4	2

1. Course Description

This course is designed to provide students with hands-on experience in front-end simulation and the implementation of digital designs using Field Programmable Gate Arrays (FPGAs). Students will learn the fundamental concepts and techniques required to design, simulate, and verify digital systems, culminating in the practical application of these designs on FPGA hardware.

2. Course Objectives:

1. To understand the basic VLSI circuits and to verify their operation.
2. Construct basic combinational circuits and verify their functionalities using EDA Tool.
3. Apply the design procedures to design basic sequential circuits using FPGA boards.
4. Understand the Design Entry & structural description using VHDL or Verilog examples.
5. To enable to design and implement finite state machines using HDL, with an emphasis on their implementation and validation on FPGA platforms.

3. Syllabus

List of Laboratory Experiments/Exercises

1. Introduction to HDL Simulation Flow.
2. Combinational circuit design using different coding styles.
3. Design an Adder (Ripple Carry / Carry Look Ahead) Multiplier (4/ 8 Bit).
4. Design and Implement Flip-Flops, Registers, and Counters.
5. Design an arithmetic logic MODULE (ALU) using HDL implement by FPGA.
6. Design Finite State Machine (Moore/Mealy) using HDL implement by FPGA.
7. Memory Subsystem Design using HDL implement by FPGA.
8. Power Aware Design of a simple subsystem.
9. Case study and Mini Project.

References:

Reference Books

1. M J Smith, "Application Specific Integrated Circuits", Addisson Wesley, 2014
2. Kishore Mishra, Advanced Chip Design, Createspace Independent Pub.

Journals:

1. https://www.sciencedirect.com/journal/microelectronics-journal
2. https://ieeexplore.ieee.org/xpl/RecentIssue.jsp?punumber=92

Video Reference:

1. https://www.youtube.com/watch?v=oZSv68esbgI
2. https://www.youtube.com/watch?v=4cPkr1VHu7Q

NPTEL Courses:

1. https://www.udemy.com/course/asic-bootcamp-sta-basic-concepts
2. https://www.coursera.org/learn/vlsi-cad-layout

4. Course Outcomes

CO. No.	Course Outcome
P23VL451.1	Understand modeling styles.
P23VL451.2	Apply modeling styles for realizing digital subsystems.
P23VL451.3	Verify and analyze HDL models by writing appropriate test benches.
P23VL451.4	Analyze the impact of coding styles on synthesis.

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P23VL451.5	Apply RTL architectures for simple digital systems.

P23VL452	ANALOG IC DESIGN LAB	L	T	P	C
		0	0	4	2

1. Course Description

This course offers a practical, hands-on approach to the design, simulation, and testing of analog integrated circuits (ICs). Students will gain experience with industry-standard design tools and methodologies, focusing on the critical aspects of analog IC design, including device modeling, circuit simulation, layout, and testing. The course is intended to complement theoretical coursework in analog electronics by providing real-world design challenges and solutions.

2. Course Objectives:

1. To understand the basic analog circuits and to verify their operation.
2. Construct current mirrors and verify their functionalities using EDA Tool.
3. Design and Implement Current Mirrors
4. Apply the design procedures to design two stage op-amps.
5. Design and Simulate Two-Stage Op-Amps

3. Syllabus

List of Laboratory Experiments/Exercises

1. Ideal Current source PMOS & NMOS
2. Single transistor amplifier
3. Cascade amplifier
4. Wilson current mirror
5. Cascade current mirror
6. Cascode current mirror
7. Regulated Cascade current mirror
8. Design and simulation of Two stage op-amps

References:

Reference Books

1. BehzadRazavi, "Design of Analog Cmos Integrated Circuits", Tata Mcgraw Hill, 2001.
2. Willey M.C. Sansen, "Analog Design Essentials", Springer, 2006.
3. Grebene, "Bipolar And Mos Analog Integrated Circuit Design", John Wiley & Sons,Inc.,2003.

Journals:

1. https://www.allaboutcircuits.com/technical-articles/what-is-analog-ic-design/
2. https://www.synopsys.com/glossary/what-is-analog-design.html

Video Reference:

1. https://www.youtube.com/watch?v=oZSv68esbgI
2. https://www.youtube.com/watch?v=4cPkr1VHu7Q

NPTEL Courses:

1. https://nptel.ac.in/courses/117105137
2. https://onlinecourses.nptel.ac.in/noc20_ee76/preview

4. Course Outcomes

CO. No.	Course Outcome
P23VL452.1	Understand the characteristics of MOS transistor.
P23VL452.2	Understand the operation of single transistor amplifier.
P23VL452.3	Verify and analyze current mirror circuits.
P23VL452.4	Design Band gap references at CMOS transistor level.
P23VL452.5	Design charge pump circuitry with phase change.

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Program Elective I

Sl. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
THEORY								
1	P23VL501	CAD for VLSI Circuits	PE	3	3	0	0	3
2	P23VL502	Advanced Digital System Design	PE	3	3	0	0	3
3	P23VL503	VLSI for IoT systems	PE	3	3	0	0	3
4	P23VL504	Electromagnetic Interference and Compatibility	PE	3	3	0	0	3

P23VL501	CAD FOR VLSI CIRCUITS	L	T	P	C
		3	0	0	3

1. Course Description

This course provides an in-depth exploration of Computer-Aided Design (CAD) tools and methodologies for Very-Large-Scale Integration (VLSI) circuit design. The course covers a comprehensive range of topics essential for the design, analysis, and optimization of VLSI circuits using advanced CAD techniques. Students will gain theoretical knowledge and practical skills necessary for designing complex integrated circuits (ICs) efficiently and effectively.

2. Course Objectives:

1. To introduce the VLSI design methodologies and design methods.
2. To introduce data structures and algorithms required for VLSI design.
3. To study algorithms for partitioning, placement, floor planning and routing.
4. To study algorithms for modeling, simulation and synthesis.
5. To introduce the integration of machine learning techniques in VLSI design

3. Syllabus

Unit-I: Introduction

Introduction to VLSI Design Methodologies – VLSI Design Cycle – New Trends in VLSI Design Cycle – Physical Design Cycle – New Trends in Physical Design Cycle – Design Styles – Review of VLSI Design Automation Tools

Unit-II: Data Structures and Basic Algorithms

Introduction to Data Structures and Algorithms – Algorithmic Graph Theory and Computational Complexity – Tractable and Intractable Problems – General Purpose Methods for Combinatorial Optimization.

Unit-III: Algorithms for Partitioning and Placement

Layout Compaction – Problem Formulation – Algorithms for Constraint Graph Compaction – Partitioning – Placement – Placement Algorithms.

Unit-IV: Algorithms for Floor Planning and Routing

Floor planning – Problem Formulation – Floor planning Algorithms – Routing – Area Routing – Global Routing – Detailed Routing.

Unit-V: Modelling, Simulation and Synthesis – Machine Learning In Synthesis

Simulation – Gate Level Modeling and Simulation – Logic Synthesis and Verification – Binary Decision Diagrams – High Level Synthesis. Machine Learning for Physical Verification, Mask Synthesis and Physical Design.

References:

Reference Books

1. Sabih H. Gerez, "Algorithms for VLSI Design Automation", Second Edition, Wiley-India, 2017.

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2. Naveed a. Sherwani, "Algorithms for VLSI Physical Design Automation", 3rd Edition, Springer, 2017.
3. Charles J. Alpert, Dinesh P. Mehta and Sachin S Sapatnekar, "Handbook of Algorithms for Physical Design Automation, CRC Press, 1st Edition, 2009.
4. N.a. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.
5. Ibrahim (Abe) M. Elfadel , Duane S. Boning and Xin Li "Machine Learning in VLSI Computer-Aided Design" Springer, 1st Edition , 2019.

Journals:

1. https://www.sciencedirect.com/journal/microelectronics-journal

Video Reference:

1. https://www.youtube.com/watch?v=O9guSe5_tG0
2. https://www.youtube.com/watch?v=5SD7QfTQs1g

NPTEL Courses:

1. https://www.vlsiguru.com/physical-design-training/
2. https://ict.iitk.ac.in/courses/vlsi-physical-design/

4. Course Outcomes

CO. No.	Course Outcome
P23VL501.1	Understand various VLSI design methodologies in Physical Design Automation.
P23VL501.2	Understand different data structures and algorithms in designing integrated circuits.
P23VL501.3	Develop algorithms for partitioning and placement in design cycle.
P23VL501.4	Develop algorithms for floor planning and routing in design cycle.
P23VL501.5	Design algorithms for modeling, simulation and synthesis.

P23VL502	ADVANCED DIGITAL SYSTEM DESIGN	L	T	P	C
		3	0	0	3

1. Course Description

This course delves into advanced concepts and methodologies in the design, implementation, and optimization of complex digital systems. Building on foundational knowledge of digital logic design, students will explore state-of-the-art techniques and tools used in the creation of sophisticated digital circuits and systems. The course covers a range of topics including high-level design methodologies, hardware description languages, system-on-chip (SoC) design, and hardware-software co-design. Through a combination of theoretical lectures and practical laboratory sessions, students will gain the skills necessary to tackle real-world digital design challenges.

2. Course Objectives:

1. To study the sequential circuit design and asynchronous sequential circuit design methods.
2. To explain the design procedures for developing complex system controllers
3. To Introduce synchronous design using programmable devices
4. To design the digital circuits using Verilog HDL.
5. To design and modeling of simple digital systems, including the datapath and control blocks, and the implementation of programmable logic devices like CPLD and FPGA

3. Syllabus

Unit-I: Combinational Circuit Design

Introduction to VLSI Design Flow - RTL Abstraction - Different Modeling Styles in Verilog - Design of Combinational Subsystems. Design of adder, subtractor, and parallel adder by Verilog HDL.

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Unit-II: Sequential Circuit Design
Sequential Building Blocks - Flip-flops – Registers - Shift Registers and Counters - State Machines. Design of Flip-Flops, Registers, and counters by Verilog HDL.
Unit-III: Asynchronous Sequential Circuit
Design of Asynchronous Sequential Circuit - Static, Dynamic, and Essential Hazards – Mixed Operating Mode Asynchronous Circuits – Design of Sequential Machines by Verilog HDL
Unit-IV: Digital Subsystem Design
Basic Aspects of Timing - Digital Subsystem Design - FIFOs - Memories - Buffers - DSP Building blocks - Word length Effects - Fixed - Floating Point Representation- Design of Serial Adders, Multiplier, and Divider by Verilog HDL
Unit-V: Design of Data Path and Control Blocks
Case Study of Design and Modeling of a Simple Digital System - Datapath and Controller Design - Programmable Logic Devices - CPLD – FPGA-Xilinx FPGA - Xilinx 4000- Design of a simple Microprocessor by Verilog HDL.
References:
Reference Books 1. Charles H.Roth Jr "Fundamentals of Logic Design" Thomson Learning, 2013 2. Michael D. Ciletti, Advanced Digital Design with Verilog HDL, Second Edition, Pearson Higher Education, 2011 3. Morris Mano and Michael D. Ciletti, Digital Design: With an Introduction to the Verilog HDL, Fifth Edition, Pearson Higher Education, 2013. 4. Donald G Givone, Digital Principles and Design, Tata McGraw Hill edition, 2012 **Journals:** 1. https://www.sciencedirect.com/journal/microelectronics-journal **Video Reference:** 1. https://onlinecourses.nptel.ac.in/noc21_ee39/preview 2. https://www.youtube.com/watch?v=g6Duh7-2-K0 **NPTEL Courses:** 1. https://www.coursera.org/learn/digital-systems 2. https://www.vlsiguru.com/advanced-digital-design-course/

4. Course Outcomes

CO. No.	Course Outcome
P23VL502.1	Analyze the combinational circuit design
P23VL502.2	Analyze the sequential circuits design
P23VL502.3	Understand the architectures for Asynchronous Sequential Circuit
P23VL502.4	Design system controllers using different digital ICs
P23VL502.5	Synthesize Data Paths and control MODULEs using Verilog HDL

P23VL503	VLSI FOR IOT SYSTEMS	L	T	P	C
		3	0	0	3

1. Course Description

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This course explores the principles and practices of Very-Large-Scale Integration (VLSI) design tailored for Internet of Things (IoT) systems. Students will gain a comprehensive understanding of how VLSI technology is used to develop efficient, low-power, and high-performance integrated circuits that are crucial for IoT applications. The course covers the entire VLSI design flow, including architecture, design, simulation, verification, and fabrication, with a specific focus on the unique requirements and challenges posed by IoT systems.

2. Course Objectives:

1. To study about basic features of IoT and to introduce the IoT paradigm
2. To study the various components and their connectivity.
3. To impart knowledge of IoT building blocks and their interactions.
4. To provide exposure to typical approaches towards IoT VLSI system implementation.
5. To study the system design and its security.

3. Syllabus

Unit-I: Introduction to Components of IOT

Introduction to IoT - Features - IoT Stack - Technologies and IoT Challenges - Concept of the connected world – Need, Legacy systems for connected world Sensors - features and limitations – Review of classic embedded system architecture, Basic building blocks of an IoT system - Sensors and Hardware for IoT- Characteristics and requirements - Connectivity technologies in IoT.

Unit-II: IC Technology for IOT

SoC architecture for IoT Devices– Application Processors, Microcontrollers, Smart Analog; Memory architecture for IoT – Non-Volatile Memories (NVM), Embedded Non-Volatile Memories, Anti-Fuse Time Programmable (OTP) memories, Power Management - Low Drop Out Regulators, DC-to-DC Converters, Voltage References, Power Management MODULEs (PMUs) in IC's and Systems, FPGA in IoT systems

Unit-III: Block Design for IOT and Cloud

Requirements, Designing Computing blocks in IoT systems - System Power Supply Design for IoT systems, Mixed Signal challenges in hardware systems, Model-based Approaches - Hardware/Software Partitioning - Computing Paradigms/Platforms - IoT/Cloud Integration.

Unit-IV: Electronic System Design for IOT

Component models & System Design – Feasibility and challenges, System Level Integration, Operating conditions of IoT devices and impact on Electronic System Design; Hardware Security issues, EMI/EMC, SI/PI, and Reliability Analysis in IoT systems

Unit-V: Security and Management

Security aspects of IoT - Integrity - Confidentiality - Authenticity - Case Study of Design of a Typical IoT System.

References:

Reference Books

1. Pethuru Raj and Anupama C. Raman, The Internet of Things: Enabling Technologies, Platforms, and Use Cases, CRC Press, 2017.
2. Adrian McEwen, Designing the Internet of Things, Wiley,2013
3. Alioto, "Enabling the Internet of Things- From Integrated Circuits to Integrated Systems", Springer Publications, First Edition, 2017.
4. Milan Milenkovic, Internet of Things: Concepts and System Design, Springer, 2020
5. Pieter Harpe, Kofi A. A. Makinwa, Andrea Baschirotto, "Hybrid ADCs, Smart Sensors for the IoT, and Sub-1V & Advanced Node Analog Circuit Design", Springer International Publishing AG, 2017
6. Jim Lipman, Sidense Corp." NVM memory: A Critical Design Consideration for IoT Applications"- https://www.design reuse.com/articles/32614/nvm-memory-iot-applications.html.

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Journals:

1. https://www.sciencedirect.com/journal/microelectronics-journal

Video Reference:

1. https://www.youtube.com/watch?v=tOikdnW_b6k

NPTEL Courses:

1. https://www.cranesvarsity.com/courses/iot-online-courses/
2. https://www.udemy.com/topic/vlsi/

4. Course Outcomes

CO. No.	Course Outcome
P23VL503.1	Understand the fundamental features of IoT and its related concepts
P23VL503.2	Ability to develop IoT abstractions for real-life problems.
P23VL503.3	Analyze various device architectures and cloud integration.
P23VL503.4	Classify the signal blocks and their interfacing
P23VL503.5	Understand system design and its security levels

P23VL504	ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY	L	T	P	C
		3	0	0	3

1. Course Description

This course provides an in-depth study of Electromagnetic Interference (EMI) and Electromagnetic Compatibility (EMC) in electronic systems. Students will explore the sources and mechanisms of EMI, methods for controlling and mitigating interference, and techniques for ensuring compatibility in complex electronic environments. The course emphasizes both theoretical concepts and practical applications, equipping students with the skills necessary to design and analyze systems for optimal electromagnetic performance.

2. Course Objectives:

1. To gain a broad conceptual understanding of the various aspects of electromagnetic interference (EM) and compatibility
2. To develop a theoretical understanding of electromagnetic shielding effectiveness
3. To understand ways of mitigating EMI by using shielding, grounding, and filtering
4. To understand the need for standards and to appreciate measurement methods
5. To study the need for EMC standards, international frameworks, measurement techniques, and testing environments.

3. Syllabus

Unit-I: Introduction & Sources of EM Interference

Introduction - Classification of sources - Natural sources - Man-made sources - Survey of the electromagnetic environment.

Unit-II: EM Shielding

Introduction - Shielding effectiveness - Far-field sources - Near-field sources - Low-frequency, magnetic field shielding - Effects of apertures.

Unit-III: Interference Control Techniques

Equipment screening - Cable screening - grounding - Power-line filters - Isolation - Balancing - Signal-line filters - Nonlinear protective devices.

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Unit-IV: EMC Standards, Measurements and Testing
Need for standards - The international framework - Human exposure limits to EM fields -EMC measurement techniques - Measurement tools - Test environments.
Unit-V: EMC Considerations In Wireless and Broadband Technologies
Efficient use of frequency spectrum - EMC, interoperability and coexistence - Specifications and alliances - Transmission of high-frequency signals over telephone and power networks – EMC and digital subscriber lines - EMC and power line telecommunications.
References:
Reference Books 1. Christopoulos C, Principles and Techniques of Electromagnetic Compatibility, CRC Press, Second Edition, Indian Edition, 2013. 2. Paul C R, Introduction to Electromagnetic Compatibility, Wiley India, Second Edition,2008. 3. Kodali V P, Engineering Electromagnetic Compatibility, Wiley India, Second Edition,2010. 4. Henry W Ott, Electromagnetic Compatibility Engineering, John Wiley & Sons Inc, Newyork,2009. 5. Scott Bennett W, Control and Measurement of Unintentional Electromagnetic Radiation, John Wiley& Sons Inc., Wiley Interscience Series, 1997. **Journals:** 1. https://www.sciencedirect.com/journal/microelectronics-journal **Video Reference:** 1. https://www.youtube.com/watch?v=Qe7p5QHVg8E&list=PLvYkIenxW1Kg3pjwmrZbh66RWU9gvUWc7 2. https://www.youtube.com/watch?v=55rgbgwFpck&list=PLyqSpQzTE6M8KHvPajlKmZDAPY_K3xb4Q **NPTEL Courses:** 1. https://archive.nptel.ac.in/courses/108/106/108106138/ 2. https://interpro.wisc.edu/courses/emc-and-best-practices/

4. Course Outcomes

CO. No.	Course Outcome
P23VL504.1	Demonstrate knowledge of the various sources of electromagnetic interference
P23VL504.2	Display an understanding of the effect of how electromagnetic fields couple through apertures, and solve simple problems based on that understanding
P23VL504.3	Explain the EMI mitigation techniques of shielding and grounding
P23VL504.4	Explain the need for standards and EMC measurement methods
P23VL504.5	Analyze the impact of EMC on wireless and broadband technologies

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Audit Course

Sl. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
THEORY								
1	P23AC901	English for Research paper writing	AC	2	2	0	0	NC
2	P23AC902	Disaster Management	AC	2	2	0	0	NC
3	P23AC903	Constitution of India	AC	2	2	0	0	NC

P23AC901	ENGLISH FOR RESEARCH PAPER WRITING	L	T	P	C
		2	0	0	NC

1. Course Description

This course is designed to equip students with the essential skills and strategies required for effective research paper writing in English. Through a combination of lectures, practical exercises, and peer reviews, students will learn the conventions of academic writing, the structure of research papers, and techniques for clear and persuasive communication of complex ideas.

2. Course Objectives:

1. Teach how to improve writing skills and level of readability
2. Tell about what to write in each section
3. Summarize the skills needed when writing a Title
4. Infer the skills needed when writing the Conclusion
5. Ensure the quality of paper at very first-time submission

3. Syllabus

Unit-I: Introduction to Research Paper Writing

Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

Unit-II: Presentation Skills

Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts, Introduction.

Unit-III: Title Writing Skills

Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.

Unit-IV: Result Writing Skills

Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions.

Unit-V: Verification Skills

Useful phrases, checking Plagiarism, how to ensure paper is as good as it could possibly be the first- time submission.

References:

Reference Books

1. Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011
2. Day R How to Write and Publish a Scientific Paper, Cambridge University Press 2006
3. Goldbort R Writing for Science, Yale University Press (available on Google Books) 2006
4. Highman N, Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book.

Journals:

1. https://link.springer.com/book/10.1007/978-3-031-31072-0

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Video Reference:

1. https://www.grammarly.com/blog/how-to-write-a-research-paper/
2. https://www.iferp.in/blog/2022/04/11/guide-to-research-paper-writing-for-non-native-english-speakers/

NPTEL Courses:

1. https://www.coursera.org/learn/academic-writing-capstone
2. https://www.udemy.com/course/how-to-write-a-successful-research-paper-academic-writing/

4. Course Outcomes

CO. No.	Course Outcome
P23AC901.1	Understand that how to improve your writing skills and level of readability
P23AC901.2	Learn about what to write in each section
P23AC901.3	Understand the skills needed when writing a Title
P23AC901.4	Understand the skills needed when writing the Conclusion
P23AC901.5	Ensure the good quality of paper at very first-time submission

P23AC902	DISASTER MANAGEMENT	L	T	P	C
		2	0	0	NC

1. Course Description

This course provides a comprehensive overview of disaster management, covering the principles, practices, and frameworks essential for effectively managing natural and human-made disasters. Students will explore the phases of disaster management—preparedness, response, recovery, and mitigation—and develop the skills needed to plan, coordinate, and execute disaster management strategies. Through case studies, simulations, and practical exercises, students will gain a deep understanding of the complexities involved in disaster scenarios and learn how to apply theoretical knowledge to real-world situations.

2. Course Objectives:

1. To Grasp the fundamental concepts, terminologies, and frameworks of disaster management.
2. To Analyze the phases of disaster management—preparedness, response, recovery, and mitigation.
3. To Identify, assess, and analyze various hazards and vulnerabilities in different contexts.
4. To Develop and implement risk management strategies to minimize the impact of disasters.
5. To understand the concept and elements of disaster risk, explore strategies for disaster risk reduction, and assess global and national efforts in risk management.

3. Syllabus

Unit-I: Introduction

Disaster: Definition, Factors and Significance; Difference between Hazard And Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude

Unit-II: Repercussions of Disasters and Hazards

Economic Damage, Loss of Human and Animal Life, Destruction Of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts

Unit-III: Disaster Prone Areas In India

Study of Seismic Zones; Areas Prone To Floods and Droughts, Landslides And Avalanches; Areas Prone To Cyclonic and Coastal Hazards with Special Reference To Tsunami; Post-Disaster Diseases and Epidemics

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Unit-IV: Disaster Preparedness and Management
Preparedness: Monitoring Of Phenomena Triggering a Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological And Other Agencies, Media Reports: Governmental and Community Preparedness
Unit-V: Risk Management
Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival
References:
Reference Books 1. Goel S. L., Disaster Administration And Management Text And Case Studies", Deep & Deep Publication Pvt. Ltd., New Delhi,2009 2. Nishitha Rai, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'New Royal book Company,2007 3. Sahni, PardeepEt.Al. ," Disaster Mitigation Experiences And Reflections", Prentice Hall Of India, New Delhi,2001 **Journals:** 1. https://www.sciencedirect.com/journal/international-journal-of-disaster-risk-reduction **Video Reference:** 1. https://www.youtube.com/watch?v=BaWnRznp1AU 2. https://www.youtube.com/watch?v=PNgsqO7w9Nk 3. https://www.ndrf.gov.in/about-us **NPTEL Courses:** 1. https://onlinecourses.swayam2.ac.in/cec19_hs20/preview 2. https://nidm.gov.in/online.asp

4. Course Outcomes

CO. No.	Course Outcome
P23AC902.1	Summarize basics of disaster
P23AC902.2	Explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.
P23AC902.3	Illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
P23AC902.4	Describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
P23AC902.5	Develop the strengths and weaknesses of disaster management approaches

P23AC903	CONSTITUTION OF INDIA	L	T	P	C
		2	0	0	NC

1. Course Description

This course offers an in-depth examination of the Constitution of India, providing students with a comprehensive understanding of its principles, structure, and functioning. It covers the historical background, the drafting process, key features, and the role of the Constitution in shaping the political, legal, and social framework of India. Through lectures, discussions, and analysis of landmark cases, students will explore the significance of the Constitution in contemporary India and its impact on governance and citizen rights.

2. Course Objectives:

1. Understand the premises informing the twin themes of liberty and freedom from a civil rights

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perspective
2. Address the growth of Indian opinion regarding modern Indian intellectuals' Constitutional Role and entitlement to civil and economic rights as well as the emergence nation hood in the early years of Indian nationalism
3. To address the role of socialism in India after the commencement of the Bolshevik Revolutionin1917and its impact on the initial drafting of the Indian Constitution.
4. To understand the roles and importance of district administration, municipalities, Panchayati Raj institutions, and elected officials at the village and block levels.
5. To explore the Election Commission's functions, the role of the Chief Election Commissioner, and other bodies dedicated to the welfare

3. Syllabus

Unit-I: The Indian Constitution – An Introduction

History, Drafting Committee, (Composition & Working), Preamble, Salient Features.

Unit-II: Contours of Constitutional Rights and Duties

Fundamental Rights, Right to Equality, Right to Freedom, Right against Exploitation, Right to Freedom of Religion, Cultural and Educational Rights, Right to Constitutional Remedies, Directive Principles of State Policy, Fundamental Duties.

Unit-III: Organs of Governance

Parliament, Composition, Qualifications and Disqualifications, Powers and Functions, Executive, President, Governor, Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualifications, Powers and Functions.

Unit-IV: Local Administration

District's Administrative head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO, Municipal Corporation. Pachayat raj: Introduction, PRI: Zila Pachayat. Elected officials and their roles, CEO Zila Pachayat: Position and role. Block level: Organizational Hierarchy(Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root democracy.

Unit-V: Election Commission

Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners - Institute and Bodies for the welfare of SC/ST/OBC and women.

References:

Reference Books

1. The Constitution of India,1950(Bare Act),Government Publication
2. Dr.S.N.Busi, Dr.B. R.Ambedkar framing of Indian Constitution,1st Edition, 2015
3. M.P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis,2014
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015

Journals:

1. https://ijcl.nalsar.ac.in/

Video Reference:

1. https://byjus.com/free-ias-prep/constitution-of-india-an-overview/
2. https://byjus.com/free-ias-prep/preamble/
3. https://www.studyiq.com/articles/salient-features-of-constitution-of-india/

NPTEL Courses:

1. https://legalaffairs.nalsar.ac.in/
2. https://www.udemy.com/course/constitution-of-india/

4. Course Outcomes

CO. No.	Course Outcome

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P23AC903.1	Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
P23AC903.2	Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India.
P23AC903.3	Discuss the circumstances surrounding the foundation of the Congress Socialist Party[CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
P23AC903.4	Discuss the passage of the Hindu Code Bill of 1956.
P23AC903.5	Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.

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Semester II

Sl. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
THEORY								
1	P23VL405	ASIC Design	PC	3	3	0	0	3
2	P23VL406	Design for Testability	PC	3	3	0	0	3
3	P23VL407	Low Power IC Design	PC	3	3	0	0	3
4	P23VL5XX	Program Elective II	PE	3	3	0	0	3
5	P23VL5XX	Program Elective III	PE	3	3	0	0	3
6	P23VL5XX	Program Elective IV	PE	3	3	0	0	3
PRACTICALS								
7	P23VL453	ASIC Design Lab	PC	4	0	0	4	2
8	P23VL454	Design for Testability Lab	PC	4	0	0	4	2
		Value Added Course	PC	2	-	-	-	-
TOTAL				**28**	**18**	**0**	**8**	**22**

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P23VL405	ASIC DESIGN	L	T	P	C
		3	0	0	3

1. Course Description

This course provides a comprehensive overview of Application-Specific Integrated Circuits (ASICs), covering their types, design flow, CMOS logic, programmable ASICs, architecture, and system-on-chip (SoC) design. Students will delve into topics such as logic synthesis, placement, routing, and explore case studies to understand practical applications in various domains, including digital cameras and high-speed data standards.

2. Course Objectives:

1. To study the ASICs design, Combinational, and Sequential CMOS logic
2. To gain knowledge of various programmable ASIC technologies, including Anti-Fuse, Static RAM, EPROM
3. Examine the architecture and configuration of modern FPGAs
4. To study Programmable ASICs, Logic Synthesis, Placement, and Routing
5. To analyse the concept of system-on-chip design

3. Syllabus

Unit-I: Introduction To ASICs, CMOS Logic and ASIC Library Design

Types of ASICs - Design flow - CMOS transistors - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort.

Unit-II: Programmable ASICS, Programmable ASIC Logic Cells and Programmable ASIC I/O Cells

Anti-Fuse - Static Ram - EPROM and EEPROM Technology - ACTEL ACT- Xilinx LCA –ALTERA FLEX - ALTERA MAX DC & AC Inputs and Outputs - Clock & Power Inputs - Xilinx I/O Blocks.

Unit-III: Programmable ASIC Architecture

Architecture and Configuration of ARTIX / Cyclone and KINTEX Ultra Scale / STRATIX FPGA – Micro-Blaze / NIOS Based Embedded Systems – Signal Probing Techniques.

Unit-IV: Logic Synthesis, Placement and Routing

Logic synthesis - ASIC floor planning- placement and routing – power and clocking strategiesLogic Synthesis - Floor Planning Goals and Objectives, Measurement of Delay in Floor Planning, Floor Planning Tools, I/O and Power Planning, Clock Planning, Placement Algorithms. Routing: Global Routing, Detailed Routing, Special Routing.

Unit-V: System-On-Chip Design

SoC Design Flow, Platform-Based and IP Based SoC Designs, Basic Concepts of Bus-Based Communication Architectures, High Performance Filters using Delta-Sigma Modulators. Case Studies: Digital Camera, SDRAM, High Speed Data standards.

References:

Reference Books

1. M J Smith, "Application Specific Integrated Circuits", Addisson Wesley, 2014
2. Steve Kilts, "Advanced FPGA Design," Wiley Inter-Science,2006
3. Roger Woods, John Mcallister, Dr. Ying Yi, Gaye Lightbod, "FPGA-Based Implementation of Signal Processing Systems", Wiley, 2008.
4. Vaibbhav Taraate, ASIC Design and Synthesis –RTL Design using Verilog, Springer, 2021.

Journals:

1. https://www.sciencedirect.com/journal/microelectronics-journal
2. https://ieeexplore.ieee.org/xpl/RecentIssue.jsp?punumber=92

Video Reference:

1. https://www.youtube.com/watch?v=oZSv68esbgI
2. https://www.youtube.com/watch?v=4cPkr1VHu7Q

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NPTEL Courses:
1. https://www.udemy.com/course/asic-bootcamp-sta-basic-concepts

4. Course Outcomes

CO. No.	Course Outcome
P23VL405.1	Apply Logical Effort Technique for predicting Delay, Delay Minimization, and FPGA Architectures
P23VL405.2	Design Logic Cells and I/O Cells
P23VL405.3	Analyze the various resources of recent FPGAs
P23VL405.4	Understand Logic Synthesis, Placement, and Routing
P23VL405.5	Analyze High-Performance Algorithms Available for ASICs

P23VL406	DESIGN FOR TESTABILITY	L	T	P	C
		3	0	0	3

1. Course Description

This course explores advanced Design for Testability (DFT) techniques for both combinational and sequential circuits, covering fault diagnosis, automatic synthesis, Built-In Self-Test (BIST), testable memory design, and self-checking circuits, equipping students with essential skills for designing reliable and efficient digital circuits.

2. Course Objectives:

1. To debug combinational and sequential logic circuits
2. To Analyze testability techniques for sequential circuits
3. To apply the concepts of BIST
4. To study fault models and test algorithms for RAMs
5. To design self-checking circuits

3. Syllabus

Unit-I: Design for Testability for Combinational Circuits

Stuck at Faults, Fault diagnosis by Path Sensitization Technique, Reed Muller's expansion technique, OR-AND-OR design, Automatic Synthesis of Testable Logic, Testable design of Multilevel Combinational Circuits.

Unit-II: Design for Testability for Sequential Circuits

Controllability and observability, Ad-Hoc Design Rules for Improving Testability, Scan Path Technique for testable Sequential Circuit design, Level Sensitive Scan Design (LSSD), Random Access Scan Technique, partial Scan, Boundary Scan.

Unit-III: Built-In Self-Test

Test Pattern generation for BIST, Output Response Analysis, Circular BIST, Built-In logic Block observer, Self-Testing using an MISR and Parallel Shift register, Sequence generator, On-Chip Self-Test.

Unit-IV: Testable Memory Design

RAM fault Models, Test Algorithms for RAMs-Galloping 0's and 1's,Walking 0's and 1's,March Test, MATS Check Board Test, Detection of Pattern-Sensitive Faults, BIST Techniques for RAM Chips.

Unit-V: Self - Checking Circuits

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Basic concepts of Self checking circuits, Design of Totally Self Checking checker- Self Checking using m/n codes, Equality Checkers, Berger code, Self-Checking Combinational Circuits, Self -Checking Sequential Circuit.
References:
Reference Books 1. Lala, Parag K. An Introduction to Logic Circuit Testing, Morgan & Claypool, 2009. 2. Parag K. Lala, Digital Circuits Testing and Testability, Academic Press, 1997. 3. M. Abramovili, M.A. Breues, A. D. Friedman, Digital Systems Testing and Testable Design, Jaico publications, 2001. 4. Zainalabedin Navabi, Digital System Test and Testable Design Using HDL Models and Architectures, Springer, 2011. **Journals:** 1. https://www.sciencedirect.com/journal/microelectronics-journal 2. https://ieeexplore.ieee.org/xpl/RecentIssue.jsp?punumber=92 **Video Reference:** 1. https://edurev.in/t/115111/Design-for-Testability-1 2. https://edurev.in/t/115116/Design-for-Testability-2 **NPTEL Courses:** 1. https://nptel.ac.in/courses/117105137 2. https://onlinecourses.nptel.ac.in/noc20_ee76/preview

4. Course Outcomes

CO. No.	Course Outcome
P23VL406.1	Describe the Testability of Combinational Circuits
P23VL406.2	Explain the Testability of Sequential Circuits
P23VL406.3	Illustrate the concepts of Built In Self-Test
P23VL406.4	Demonstrate the design for Testability of Memory Circuits
P23VL406.5	Illustrate Self Checking Circuits using various techniques

P23VL407	LOW-POWER IC DESIGN	L	T	P	C
		3	0	0	3

1. Course Description

This course delves into power dissipation in CMOS circuits and explores strategies for low-power design across hierarchy levels. Topics include power optimization techniques, design of low-power CMOS circuits, power estimation methods, and synthesis and software design tailored for low-power requirements, providing essential skills for designing energy-efficient VLSI systems.

2. Course Objectives:

1. Identify sources of power in an IC.
2. Identify the power reduction techniques based on technology-independent and technology-dependent methods.
3. Identify suitable techniques to reduce power dissipation.
4. Estimate power dissipation of various MOS logic circuits and develop an algorithm for low power dissipation.

3. Syllabus

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Unit-I: Power Dissipation in CMOS
Hierarchy of Limits of Power – Sources of Power Consumption – Physics of Power Dissipation in CMOS FET Devices – Basic Principle of Low Power Design.
Unit-II: Power Optimization
Logic Level Power Optimization – Circuit Level Low Power Design – Gate Level Low Power Design – Architecture Level Low Power Design – VLSI Subsystem Design of Adders, Multipliers, PLL, Low Power Design.
Unit-III: Design of Low-Power CMOS Circuits
Computer Arithmetic Techniques for Low Power System – Reducing Power Consumption in Combinational Logic, Sequential Logic, Memories – Low Power Clock – Advanced Techniques –Special Techniques, Adiabatic Techniques – Physical Design, Floor Planning, Placement, and Routing.
Unit-IV: Power Estimation
Power Estimation Techniques, Circuit Level, Gate Level, Architecture Level, Behavioral Level, – Logic Power Estimation – Simulation Power Analysis –Probabilistic Power Analysis.
Unit-V: Synthesis and Software Design for Low Power
Synthesis for Low Power – Behavioral Level Transform –Algorithms for Low Power – Software Design for Low Power.
References:
Reference Books 1. Kaushik Roy, Sharat Prasad, "Low power CMOS VLSI circuit design", John Wiley's sonsInc.,2000. 2. J.B.Kulo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley, 1999. 3. James B.Kulo, Shih-Chia Lin, "Low Voltage SOI CMOS VLSI Devices and Circuits", John Wiley and Sons, Inc. 2001 4. J.Rabaey, "Low Power Design Essentials (Integrated Circuits and Systems)", Springer, 2009. **Journals:** 1. https://www.sciencedirect.com/journal/microelectronics-journal 2. https://ieeexplore.ieee.org/xpl/RecentIssue.jsp?punumber=92 **Video Reference:** 1. https://resources.system-analysis.cadence.com/blog/msa2021-low-power-design-techniques-for powerintegrity-in-vlsi 2. https://www.synopsys.com/glossary/what-is-low-power-design.html **NPTEL Courses:** 1. https://nptel.ac.in/courses/106105034 2. https://www.vlsiguru.com/low-power-pavan/

4. Course Outcomes

CO. No.	Course Outcome
P23VL407.1	Understand the power dissipation of MOS circuits
P23VL407.2	Design and analyze various MOS logic circuits
P23VL407.3	Apply low-power techniques for low-power dissipation
P23VL407.4	Explain the power dissipation estimation of ICs
P23VL407.5	Develop algorithms to reduce power dissipation by software

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P23VL453	ASIC DESIGN LABORATORY	L	T	P	C
		0	0	4	2

1. Course Description

This course offers hands-on experiments covering RTL design, FSM design and verification, logic design synthesis, gate-level simulation, basic static timing analysis, power analysis using Cadence tools, and introductory placement and routing using Cadence software. Students gain practical experience in designing, verifying, and analysing digital circuits, essential for understanding and implementing complex VLSI systems.

2. Course Objectives:

1. To learn of basic design approaches of Application Specific Integrated Circuits
2. To finally come out with practical knowledge of doing tapeout.

3. Syllabus

List of Laboratory Experiments/Exercises

1. Register Transfer Level (RTL) Design: Implementation, Simulation, and Verification of Digital Circuits.
2. Finite State Machine (FSM) Design and Verification: Practical Implementation, Simulation, and Validation of Sequential Circuits.
3. Logic Design Synthesis and Gate-Level Simulation: Optimization, and Analysis of Digital Circuits.
4. Fundamental Exploration of Static Timing Analysis: Timing Constraints, Paths, and Optimization Techniques for ASICs.
5. Power Analysis Techniques using CADENCE: Power Consumption, Leakage, and Optimization Strategies.
6. Placement and Routing Techniques using CADENCE: Optimization, and Analysis of Physical Design

References:

Reference Books

1. M J Smith, "Application Specific Integrated Circuits", Addisson Wesley, 2014
2. Kishore Mishra, Advanced Chip Design, Createspace Independent Pub.

Journals:

1. https://www.sciencedirect.com/journal/microelectronics-journal
2. https://ieeexplore.ieee.org/xpl/RecentIssue.jsp?punumber=92

Video Reference:

1. https://www.youtube.com/watch?v=oZSv68esbgI
2. https://www.youtube.com/watch?v=4cPkr1VHu7Q

NPTEL Courses:

1. https://www.udemy.com/course/asic-bootcamp-sta-basic-concepts
2. https://www.coursera.org/learn/vlsi-cad-layout

4. Course Outcomes

CO. No.	Course Outcome
P23VL453.1	To well versed with the ASIC design flow used in IC design using industry standard EDA tools
P23VL453.2	Learning the designing skill of Finite state machine used in complex digital design using HDL
P23VL453.3	Preform synthesis of the design, generate the gate level netlist and report the area, timing and Power analysis
P23VL453.4	Perform the gate level simulation, placement and routing of design using EDA Tools.
P23VL453.5	Preform the hands-on practice of creating ICs with the knowledge of IC design flow and using industry standard EDA Tools.

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P23VL454	DESIGN FOR TESTABILITY LABORATORY	L	T	P	C
		0	0	4	2

1. Course Description

This course focuses on practical implementation and testing aspects of digital designs, covering topics such as packet and class implementation, driver development, line and code coverage analysis for counters and FSMs, functional coverage and code coverage analysis for ALUs, and bus function model generation and testing. Through hands-on exercises, students gain proficiency in designing, testing, and analysing various components of digital circuits, preparing them for real-world VLSI development tasks.

2. Course Objectives:

1. To test and verify the functionality of simple DUT
2. To perform code coverage for a FSM / DUT

3. Syllabus

List of Laboratory Experiments/Exercises

1. Implementation and verification of packet and class structures for a simple Design Under Test (DUT).
2. Design and implementation of a driver module for a basic Design Under Test (DUT).
3. Analysis and evaluation of line and code coverage for a counter design.
4. Investigation and assessment of line and code coverage for a Finite State Machine (FSM) design.
5. Analysis of functional and code coverage for an Arithmetic Logic Unit (ALU) design.
6. Test Generation of bus function models for a basic Design Under Test (DUT).

References:

Reference Books

1. Lala, Parag K. An Introduction to Logic Circuit Testing, Morgan & Claypool, 2009.
2. Parag K. Lala, Digital Circuits Testing and Testability, Academic Press, 1997.

Journals:

1. https://www.sciencedirect.com/journal/microelectronics-journal
2. https://ieeexplore.ieee.org/xpl/RecentIssue.jsp?punumber=92

Video Reference:

1. https://edurev.in/t/115111/Design-for-Testability-1
2. https://edurev.in/t/115116/Design-for-Testability-2

NPTEL Courses:

1. https://nptel.ac.in/courses/117105137
2. https://onlinecourses.nptel.ac.in/noc20_ee76/preview

4. Course Outcomes

CO. No.	Course Outcome
P23VL454.1	Develop packet, class, and driver for a DUT
P23VL454.2	Analyze line, code and functional coverage
P23VL454.3	Examine the assertions for DUT
P23VL454.4	Functional verification of a FSM.
P23VL454.5	Develop a simple DUT and test the functionality

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Program Elective II

Sl. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
THEORY								
1	P23VL506	Hardware Design and Verification Languages	PE	3	3	0	0	3
2	P23VL505	VLSI Signal Processing	PE	3	3	0	0	3
3	P23VL507	DSP Processor Architecture and Programming	PE	3	3	0	0	3
4	P23VL508	Hardware Software Co-Design for FPGA	PE	3	3	0	0	3

P23VL506	HARDWARE DESIGN AND VERIFICATION LANGUAGES	L	T	P	C
		3	0	0	3

1. Course Description

System Verilog is used to model complex digital logic and verify the correctness of hardware designs. This hardware verification language is used to model, design, simulate, test and implement electronic systems. It is used to understand the functional verification process and its different methodologies. It also emphasizes the need and use of reusable verification environments using UVM.

2. Course Objectives:

1. To understand the functional verification and its different methodologies.
2. To learn the Data types, Procedural statements and Routines in system Verilog
3. To understand the Verification environment using System Verilog.
4. To develop reusable verification environment using UVM

3. Syllabus

Unit-I: Verification Techniques

Introduction to Verification - Testing Vs Verification - Verification Technologies – Functional Verification- Code coverage – Functional coverage. Testbench – Linear Testbench - Linear Random Testbench - Self-checking Testbench – Regression - RTL Formal Verification

Unit-II: System Verilog – Data Types

Introduction to System Verilog – Literal values-data Types – Arrays – Array methods – Creating new types with typedef – user defined structures – Enumerated types – attributes - operators – expressions

Unit-III: Procedural statements and Routines

Procedural statements and control flow - Processes in System Verilog – Task and functions – Routine arguments – Returning from a routine.

Unit-IV: Connecting Testbench and Design

Separating the Testbench and Design - The Interface Construct - Stimulus Timing - Interface Driving and Sampling - Program Block Consideration - Connecting together System Verilog Assertions

Unit-V: Universal Verification Methodology

Introduction to UVM - Verification components - Transaction level modelling - Developing reusable verification components - Using Verification components – Developing reusable verification environment

Text Books:

1. Christian B Spear, "System Verilog for Verification: A guide to learning the Testbench language features", Springer publications, Third Edition, 2012.
2. Vanessa R. Copper, "Getting started with UVM: A Beginner's Guide", Verilab Publishing, First Edition, 2013.

References:

Reference Books

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1. Ray Salmei, "The UVM Primer: A Step-by-Step Introduction to the Universal Verification Methodology" Boston Light Press; First edition, 2013.
2. Janick Bergeron, "Writing Testbenches using System Verilog" Synopsys Inc., Springer Publications, 2006.

Journals:

1. https://www.sciencedirect.com/journal/microprocessors-and-microsystems
2. https://www.sciencedirect.com/journal/aeu-international-journal-of-electronics-and-communications

Video Reference:

1. https://www.youtube.com/watch?v=5LUQxIDRsRI

NPTEL Courses:

1. https://onlinecourses.nptel.ac.in/noc21_ee97/preview
2. https://onlinecourses.nptel.ac.in/noc22_cs94/preview

4. Course Outcomes

CO. No.	Course Outcome
P23VL506.1	Understand the process of functional verification and its different methodologies.
P23VL506.2	Apply HDL such as System Verilog for different digital VLSI systems.
P23VL506.3	Analyze the Procedural statements and Routines in System Verilog.
P23VL506.4	Understand the Verification environment using System Verilog.
P23VL506.5	Model the reusable verification environment using UVM.

P23VL505	VLSI SIGNAL PROCESSING	L	T	P	C
		3	0	0	3

1. Course Description

VLSI (Very Large Scale Integration) Signal Processing is an advanced course designed to provide students with a comprehensive understanding of signal processing techniques and their implementation in VLSI circuits. The course explores the intersection of signal processing theory and VLSI design methodologies, focusing on the integration of algorithms and hardware for efficient signal processing systems.

2. Course Objectives:

1. To understand the principles of signal processing and their application in VLSI design.
2. To learn various VLSI architectures and design methodologies for efficient signal processing.
3. To gain hands-on experience in designing, simulating, and optimizing VLSI signal processing circuits.
4. To explore advanced topics and emerging trends in VLSI signal processing research and industry applications.

3. Syllabus

Unit-I: Introduction to DSP Systems

Typical DSP Algorithms - DSP Application Demands and Scaled CMOS Technologies - Representations of DSP Algorithms - Data-Flow Graph Representations.

Unit-II: Pipelining, Parallel processing and Retiming

Pipelining and Parallel Processing - Introduction to Retiming - Definitions and Properties - Solving Systems of Inequalities - The Bellman-Ford Algorithm - The Floyd Warshall Algorithm- Retiming Techniques.

Unit-III: Unfolding

Introduction, An Algorithm for Unfolding, Properties of Unfolding, Critical Path, Unfolding, and Retiming, Applications of Unfolding.

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Unit-IV: Folding
Introduction, Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures.
Unit-V: Scaling and Rounding Noise
Introduction, Scaling and Rounding Noise, State Variable Description of Digital Filters, Scaling and Rounding Noise Computation, Rounding Noise in Pipelined IIR Filters.
Text Books:
1. KeshabK.Parhi, VLSI Digital Signal Processing Systems: Design and Implementation, Reprint,Wiley, Inter Science, 2014. 2. John G. Proakis, Dimitris K Manolakis, Digital Signal Processing: Principles, Algorithms and Applications, Prentice Hall, Fourth Edition, 2015.
References:
Reference Books: 1. Mohammed Ismail and Terri Fiez, Analog VLSI Signal and Information Processing, McGraw-Hill, 2014. 2. S.Y. Kung, H.J. White House, T. Kailath, VLSI and Modern Signal Processing, PHI, 2010. **Journals:** 1. https://link.springer.com/journal/11265 2. https://matjournals.com/Journal-of-VLSI-Design-and-Signal-Processing.html **Video Reference:** 1. https://www.youtube.com/watch?v=gIgNlhuqxWo **NPTEL Courses:** 1. https://www.youtube.com/watch?v=ZWBs76k3GXI

4. Course Outcomes

CO. No.	Course Outcome
P23VL505.1	Compare various representation methods of DSP algorithms
P23VL505.2	Apply pipelining and parallel processing techniques to alter FIR structures for efficiency
P23VL505.3	Analyze the unfolding algorithm in software with loop optimization techniques.
P23VL505.4	Analyze the trade-offs involved in choosing between time folding and space folding based on application requirements.
P23VL505.5	Understand the Impact of Scaling and Rounding Noise

P23VL507	DSP PROCESSOR ARCHITECTURE AND PROGRAMMING	L	T	P	C
		3	0	0	3

1. Course Description

Digital signal processor is a specialized microprocessor chip designed with an architecture specifically tailored for the computational demands of digital signal processing tasks. DSPs find extensive application in various fields including audio signal processing, telecommunications, digital image processing, radar, sonar, and speech recognition systems. The primary objective of a DSP is to analyze, filter, or compress continuous real-world analog signals into digital format for further processing or transmission.

2. Course Objectives:

1. To understand the fundamentals of DSP integrated circuits and architectures.
2. To synthesize DSP architectures by applying top-down approach.
3. To apply the interfacing of Memory, I/O, and CODEC to DSP Processors.
4. To compare the features and performance of Advanced DSP devices and design filters.

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3. Syllabus

Unit-I: DSP INTEGRATED CIRCUITS AND ARCHITECTURES

Standard digital signal processors – Application-specific ICs for DSP - DSP systems - DSP system design - Integrated circuit design. DSP Computational Building Blocks - Bus Architecture and Memory - Data Addressing Capabilities - Address Generation Unit - Programmability and Program Execution - Features for External Interfacing.

Unit-II: SYNTHESIS OF DSP ARCHITECTURES

A top-down approach to DSP LSI - Circuit Synthesis – High-Performance Data conversion Techniques - LSI Algorithms and Architectures - Hierarchical Design of Processor Arrays - Systolic Arrays - Stack Filters - Wave-front Array Processors.

Unit-III: DSP PROCESSORS INTERFACING

External bus interfacing signals - Memory interface - Parallel I/O interface - Programmed I/O -Interrupts and I/O -Direct memory access (DMA) A Multichannel buffered serial port (McBSP) - McBSP Programming. Interfacing CODEC- Architectures of Multiprocessors-Performance comparison of - Multiprocessor Structures.

Unit-IV: ADSP PROCESSORS

The architecture of ADSP-21XX and ADSP-210XX series of DSP processors- Addressing modes and assembly language instructions – Application programs –Filter design, FFT calculation.

Unit-V: APPLICATIONS OF PROGRAMMABLE DSP DEVICES

DSP-Based Biotelemetry Receiver - A Speech Processing System - An Image Processing System - A Position Control System for a Hard Disk Drive - DSP-Based Power Meter

Text Books:

1. Avtar Singh and S. Srinivasan, Digital Signal Processing – Implementations using DSP Microprocessors with Examples from TMS320C54xx, Cengage Learning India Private Limited, Delhi 2012
2. Lars Wanhammer, DSP Integrated Circuits, Academic press, New York, 2011

References:

Reference Books

1. Rulph Chassaing, Digital Signal Processing and Applications with the C6713 and C6416 DSK, A John Wiley & Sons, Inc., Publication, 2005.
2. B.Venkataramani and M.Bhaskar, "Digital Signal Processors – Architecture, Programming and Applications" – Tata McGraw – Hill Publishing Company Limited. New Delhi, 2003.Publications, 2006.

Journals:

1. https://www.tandfonline.com/action/journalInformation?show=aimsScope&journalCode=tetn20
2. https://www.sciencedirect.com/journal/aeu-international-journal-of-electronics-and-communications

Video Reference:

1. https://www.youtube.com/watch?v=VNJidtzauu8
2. https://www.youtube.com/watch?v=0Y78c9cLdvA

NPTEL Courses:

1. https://nptel.ac.in/courses/108106149
2. https://archive.nptel.ac.in/courses/108/108/108108185/

4. Course Outcomes

CO. No.	Course Outcome
P23VL507.1	Understand the fundamentals of DSP integrated circuits and architectures
P23VL507.2	Analyze the DSP architectures by applying the top-down approach to solve DSP algorithms

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P23VL507.3	Understand interfacing of Memory, I/O, and CODEC to DSP Processors.
P23VL507.4	Analyze the ADSP architectures by applying the top-down approach to solve DSP algorithms
P23VL507.5	Identify the applications of programmable DSP devices.

P23VL508	HARDWARE SOFTWARE CO-DESIGN FOR FPGA	L	T	P	C
		3	0	0	3

1. Course Description

This course provides an introduction to the design of electronic systems that incorporate both hardware and software components. Techniques for modeling hardware and software components at different levels of abstraction and at their interfaces are investigated.

2. Course Objectives:

1. To acquire knowledge about system specification and modeling
2. To learn the formulation of partitioning
3. To study the different technical aspects of prototyping and emulation

3. Syllabus

Unit-I: SYSTEM SPECIFICATION AND MODELLING: 9

Embedded Systems, Hardware/Software Co-Design, Co-Design for System Specification and Modeling, Co-Design for Heterogeneous Implementation - Processor Synthesis, Single-Processor Architectures with One ASIC, Single-Processor Architectures with Many ASICs, Multi-Processor Architectures, Comparison of Co-Design Approaches, Models of Computation, Requirements for Embedded System Specification.

Unit-II: HARDWARE/SOFTWARE PARTITIONING: 9

The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of The Partitioning Graph, Formulation of The HW/SW Partitioning Problem, Optimization, HW/SW Partitioning Based On Heuristic Scheduling, HW/SW Partitioning Based On Genetic Algorithms.

Unit-III: HARDWARE/SOFTWARE CO-SYNTHESIS: 9

The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis.

Unit-IV: PROTOTYPING AND EMULATION: 9

Introduction, Prototyping and Emulation Techniques, Prototyping and Emulation Environments, Future Developments in Emulation and Prototyping, Target Architecture, Architecture Specialization Techniques, System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data-Dominated Systems, Mixed Systems and Less Specialized Systems.

Unit-V: DESIGN SPECIFICATION AND VERIFICATION: 9

Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification, Languages for System-Level Specification and Design System-Level Specification, Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Co-Simulation.

Text Books:

1. Patrick Schaumont, "A Practical Introduction to Hardware/Software Co-design", Springer,2010
2. Ralf Niemann, "Hardware/Software Co-Design for Data Flow Dominated Embedded Systems", Kluwer Academic Publisher, 1998.

References:

Reference Books

1. Jorgen Staunstrup, Wayne Wolf, "Hardware/Software Co-Design: Principles and Practice", Kluwer Academic Publisher,1997

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2. Giovanni De Micheli, Rolf Ernst Morgon, "Reading in Hardware/Software Co-Design", Kaufmann Publisher,2001

Journals:

1. J. M. Saul, "Hardware/software codesign for FPGA-based systems," Proceedings of the 32nd Annual Hawaii International Conference on Systems Sciences. 1999. HICSS-32. Abstracts and CD-ROM of Full Papers, Maui, HI, USA, 1999, pp. 10 doi: 10.1109/HICSS.1999.772879

Video Reference:

1. https://www.youtube.com/watch?v=M-5uJe2ctRQ
2. https://www.youtube.com/watch?v=w-KHW7ZxMW8

NPTEL Courses:

1. https://nptel.ac.in/courses/106105159

4. Course Outcomes

CO. No.	Course Outcome
P23VL508.1	Describe The Broad Range of System Architectures and Design Methodologies that currently exist and define their fundamental attributes
P23VL508.2	Discuss the Dataflow Models as a State-of-the-Art Methodology to Solve Co-Design Problems and Optimize the balance between Software and Hardware
P23VL508.3	Understand Translating between Software and Hardware Descriptions through Co-Design Methodologies
P23VL508.4	Understand the State-of-The-Art practices in developing Co-Design Solutions to problems using modern Hardware/Software Tools for building prototypes
P23VL508.5	Understand the Concurrent Specification from an Algorithm, analyze its behavior, and partition the Specification into Software (C Code) and Hardware (HDL) Components

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Program Elective III

Sl.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
THEORY								
1	P23VL509	Scripting Languages for VLSI	PE	3	3	0	0	3
2	P23VL510	VLSI for Wireless Communication	PE	3	3	0	0	3
3	P23VL511	Soft Computing and Optimization Techniques	PE	3	3	0	0	3
4	P23VL512	Reconfigurable Architectures	PE	3	3	0	0	3

P23VL509	SCRIPTING LANGUAGES FOR VLSI	L	T	P	C
		3	0	0	3

1. Course Description

A scripting language is a programming language that tells the computer what exactly to do in terms of a specific script or a language. They not only make your work faster but also can make your job easier. Scripting languages can range from highly domain-specific languages to general-purpose programming languages. The use of scripting language is not just limited to a specific domain, it can be used in any programming environment that requires the user to do a repeated manual effort and script automates.

2. Course Objectives:

1. Provide an overview of scripting languages commonly used in VLSI design
2. To study the principles of Scripting Languages like Perl, TCL and Python.
3. To write the scripts for automation using the languages like Perl, TCL and Python

3. Syllabus

Unit-I: Introduction to Scripting and PERL

Characteristics of scripting languages, Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data, working with arrays, Lists and hashes, Simple input and output, Strings.

Unit-II: Advanced PERL

Finer points of Looping, Subroutines, Using Pack and Unpack, working with files, Navigating the file system, Type globs, Eval, References, Data structures, Packages, Libraries and modules, Objects, Objects and modules in action.

Unit-III: TCL

The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes.

Unit-IV: Advanced TCL

The eval, source, exec and up-level commands, Libraries and packages, Namespaces, trapping errors, Event-driven programs, making applications 'Internet-aware', 'Nuts-and-bolts' internet programming, Security issues.

Unit-V: Python Programming

Introduction to Python, Using Python interpreter, Control flow Tools, Data structures, Modules, Input and Output – Errors and Exceptions.

Text Books:

1. Brent Welch,"Practical Programming in TCL and TK",Fourth Edition, 2003
2. David Barron, "The World of Scripting Languages", Wiley Publications, 2000.

References:

Reference Books

1. Guido van Rossum, and Fred L. Drake ", Python Tutorial, Jr., editor, Release 2.6.4.,2010

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2. Randal L. Schwartz, "Learning PERL", Sixth Edition, O'Reilly, 2011.

Journals:

1. ACM Transactions on Programming Languages and Systems
2. Journal of Programming Languages

Video Reference:

1. https://www.oreilly.com/library/view/learning-perl-6th/9781449311-63/ch-1.htm
2. https://www.eyrolles.com/Informatique/Livre/practical-programming-in-tcl-and-tk-978-1361683--/l

NPTEL Courses:

1. Introduction to Perl
2. https://www.udemy.com/course/vsd-tcl-programming-from-novice-to-expert/

4. Course Outcomes

CO. No.	Course Outcome
P23VL509.1	Understand scripting language environment.
P23VL509.2	Develop the PERL scripts
P23VL509.3	Apply the TCL & TK scripts for automation
P23VL509.4	Analyse the python scripts for automation
P23VL509.5	Write scripts for a given EDA design automation

P23VL510	VLSI FOR WIRELESS COMMUNICATION	L	T	P	C
		3	0	0	3

1. Course Description

The realm of digital data like text, the integration of intricate error-tolerant communication protocols into single VLSI devices proves advantageous. In 5G telecommunications, where achieving data rates surpassing tens of gigabits per second demands specialized Application-Specific Integrated Circuits. This convergence of communication and computer systems surpasses mere recognition of individual fields, highlighting their interconnectedness. To advance such ground breaking technologies, significant focus must be placed on crafting efficient VLSI architectures.

2. Course Objectives:

1. To understand the fundamentals of Communication Concepts
2. To learn the Coding theory algorithms and Transceiver architectures
3. To understand the OFDM system and LDPC coding algorithms
4. To study the Analog impairment and its issues

3. Syllabus

Unit-I: Basic Communication Concepts

Introduction- Modulation schemes- Classical channels- Wireless channel description- Path loss- Multipath fading- channel model & envelope fading- frequency selective.

Unit-II: Coding Theory Algorithms and Architecture

Convolution codes- trellis diagram- Viterbi algorithm- soft input decoding- soft output decoding- Turbo codes- LDPC coding- concatenated convolution codes- weight distribution- Space-Time codes- spatial channels- performance measure- Orthogonal space-time block codes- spatial multiplexing.

Unit-III: Transceiver Architecture and Issues

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Receiver Architectures- Super heterodyne receiver- Image rejection receiver--Hartley and Weaver- Zero IF receiver- Low IF receiver- Transmitter architecture- Super heterodyne transmitter- Direct up transmitter- Two-step-up transmitter- Transceiver architectures for modern wireless systems- Case study- LNA- comparison of narrowband and wideband LNA- Wideband LNA design- Narrow band LNA- impedance matching and core amplifier.

Unit-IV: OFDM System

Convolution codes- trellis diagram- Viterbi algorithm- soft input decoding- soft output decoding- Turbo codes- LDPC coding- concatenated convolution codes- weight distribution- Space-Time codes- spatial channels- performance measure- Orthogonal space-time block codes- spatial multiplexing.

Unit-V: Analog Impairment and Issues

Receiver sensitivity and noise figure- DC offsets- LO leakage- Receiver interferers and intermodulation distortion- Image rejection- Quadrature balance and relation to Image rejection- relation to EVM, Peak to average power ratio- Local oscillator pulling in PLL- effect of phase noise in PLL- Effect of phase noise on OFDM systems- Effect of frequency errors on OFDM systems.

Text Books:

1. Pui-In Mak, Seng-Pan U, Rui Paulo Martins, "Analog-Baseband Architectures and Circuits for Multistandard and Low Voltage Wireless transceivers", Springer, 2007.
2. Emad N. Farag, Mohamed I. Elmasry, "Mixed signal VLSI Wireless Design Circuits and Systems", Kluwer Academic Publishers, 2002.

References:

Reference Books:

1. Andre Neubauer, Jurgen Freudenberger, Volker Kuhn, "Coding Theory, Algorithms, Architectures and Applications", John Wiley & S
2. Wolfgang Eberle, "Wireless Transceiver Systems Design", Springer, 2008.

Journals:

1. https://link.springer.com/journal/11276
2. https://www.sciencedirect.com/journal/aeu-international-journal-of-electronics-and-communications

Video Reference:

1. https://www.youtube.com/watch?v=wHsBLg8kEDE
2. https://www.youtube.com/watch?v=cRSj4FzdXfo&list=PLw-fM2uDN4J6j7DYaJuq7U2YBDXQoJdEU

NPTEL Courses:

1. https://nptel.ac.in/courses/106106167
2. https://onlinecourses.nptel.ac.in/noc24_ee63/preview

4. Course Outcomes

CO. No.	Course Outcome
P23VL510.1	Understand the fundamentals of modulation schemes, fading concepts in communication system
P23VL510.2	Analyze the Coding theory algorithms and their architectures
P23VL510.3	Understand the various Transceiver architectures and their issues.
P23VL510.4	Examine the OFDM system and LDPC coding algorithms
P23VL510.5	Identify the Analog impairment and their issues

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P23VL511	SOFT COMPUTING & OPTIMIZATION TECHNIQUES	L	T	P	C
		3	0	0	3

1. Course Description

This course will cover fundamental concepts used in soft computing. The concepts of Fuzzy logic (FL) will be covered first, followed by Artificial Neural Networks (ANNs) and optimization techniques using Genetic Algorithm (GA). Applications of Soft Computing techniques to solve a number of real-life problems will be covered to have hands on practices. In summary, this course will provide exposure to theory as well as practical systems and software used in soft computing.

2. Course Objectives:

1. To solve single-objective optimization problems using Gas.
2. To solve multi-objective optimization problems using Evolutionary algorithms (MOEAs).
3. To study the Applications of Soft computing to solve problems in varieties of application domains.

3. Syllabus

Unit-I: Introduction to Soft Computing

Concept of computing systems - Soft" computing versus "Hard" computing -Characteristics of Soft computing - Some applications of Soft computing techniques

Unit-II: Fuzzy Logic

Introduction to Fuzzy logic - Fuzzy sets and membership functions - Operations on Fuzzy sets - Fuzzy relations, rules, propositions, implications and inferences. Defuzzification techniques - Fuzzy logic controller design - Some applications of Fuzzy logic.

Unit-III: Genetic Algorithms

Concept of "Genetics" and "Evolution" and its application to probabilistic search techniques - Basic GA framework and different GA architectures - GA operators: Encoding, Crossover, Selection, Mutation, etc. - Solving single-objective optimization problems using GAs.

Unit-IV: Multi-Objective Optimization Problem Solving

Concept of multi-objective optimization problems (MOOPs) and issues of solving them - Multi-Objective Evolutionary Algorithm (MOEA) - Non-Pareto approaches to solve MOOPs - Pareto-based approaches to solve MOOPs -Some applications with MOEAs.

Unit-V: Artificial Neural Networks

Biological neurons and its working - Simulation of biological neurons to problem solving - Different ANNs architectures - Training techniques for ANNs - Applications of ANNs to solve some real-life problems.

Text Books:

1. Fuzzy Logic: A Pratical approach, F. Martin, Mc Neill, and Ellen Thro, AP Professional, 2000.
2. Fuzzy Logic with Engineering Applications (3rd Edition.), Timothy J. Ross, Willey, 2010.
3. Foundations of Neural Networks, Fuzzy Systems, and Knowldge Engineering, Nikola K. Kasabov, MIT Press, 1998.
4. Fuzzy Logic for Embedded Systems Applications, Ahmed M. Ibrahim, Elesvier Press, 2004.

References:

Reference Books:

1. An Introduction to Genetic Algorithms, Melanie Mitchell, MIT Press, 2000.
2. Genetic Algorithms in Search, Optimization and Machine Learning, David E. Goldberg, Pearson Education, 2002.
3. Practical Genetic Algorithms, Randy L. Haupt and sue Ellen Haupt, John Willey & Sons, 2002.
4. Neural Networks, Fuzzy Logis and Genetic Algorithms: Synthesis, and Applications, S. Rajasekaran, and G. A. Vijayalakshmi Pai, Prentice Hall of India, 2007.
5. Soft Computing, D. K. Pratihar, Narosa, 2008.
6. Neuro-Fuzzy and soft Computing, J.-S. R. Jang, C.-T. Sun, and E. Mizutani, PHI Learning, 2009.
7. Neural Networks and Learning Machines, (3rd Edn.), Simon Haykin, PHI Learning, 2011.

Journals:

1. https://www.ieeesmc.org/technical-activities/cybernetics/soft-computing/

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2. https://cis.ieee.org/publications/t-fuzzy-systems

Video Reference:

1. https://www.youtube.com/watch?v=pcMi89GscwM

NPTEL Courses:

1. https://onlinecourses.nptel.ac.in/noc22_cs54/preview

4. Course Outcomes

CO. No.	Course Outcome
P23VL511.1	Understand Fuzzy logic and its applications.
P23VL511.2	Understand Artificial neural networks and its applications.
P23VL511.3	Analyse single-objective optimization problems using GAs.
P23VL511.4	Analyse multi-objective optimization problems using Evolutionary algorithms (MOEAs).
P23VL511.5	Understand applications of soft computing to solve problems in varieties of application domains.

P23VL512	RECONFIGURABLE ARCHITECTURES	L	T	P	C
		3	0	0	3

1. Course Description

The course on Reconfigurable Architectures provides students with a comprehensive understanding of the principles, design methodologies, and applications of reconfigurable computing systems. The course covers theoretical concepts on efficient hardware solutions for various applications.

2. Course Objectives:

1. The student shall develop an overview and deeper insight into the research and development that is underway to meet the future needs of flexible processors
2. To learn the concepts of implementation, synthesis, and placement of modules in reconfigurable architectures
3. To understand the communication techniques and System on Programmable Chips for reconfigurable architectures
4. To learn the process of reconfiguration management

3. Syllabus

Unit-I: INTRODUCTION TO RECONFIGURATION

General purpose computing – domain specific processors –Application Specific Processors– reconfigurable computing – fields of application – evolution of reconfigurable systems – simple Programmable Logic Devices – Complex Programmable Logic Devices – Field Programmable Gate Arrays – coarse-grained reconfigurable devices.

Unit-II: IMPLEMENTATION, SYNTHESIS AND PLACEMENT

Integration – FPGA design flow – logic synthesis – LUT based technology mapping – modeling – temporal partitioning algorithms – offline and online temporal placement – managing device's free and occupied spaces.

Unit-III: COMMUNICATION AND SOPC

Direct communication – communication over third party – bus based communication – circuit switching – Network on Chip – dynamic Network on Chip – System on a Programmable Chip – adaptive multi-processing on chip.

Unit-IV: RECONFIGURATION MANAGEMENT

Reconfiguration – configuration architectures – managing the reconfiguration process – reducing configuration transfer time – configuration security.

Unit-V: APPLICATIONS OF PROGRAMMABLE HARDWARES

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FPGA based parallel pattern matching - low power FPGA based architecture for microphone arrays in Wireless Sensor Networks - exploiting partial reconfiguration on a dynamic coarse grained reconfigurable architecture – parallel pipelined OFDM baseband modulator with dynamic frequency scaling for 5G systems.

Text Books:

1. Christophe Bobda, "Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications", Springer 2007.
2. Scott Hauck and Andre Dehon, "Reconfigurable Computing: The Theory and Practice of FPGA Based Computation", Elsevier 2008.

References:

Reference Books

1. M.Gokhale and P. Graham, "Reconfigurable Computing: Accelerating Computation with Field-Programmable Arrays", Springer, 2005.
2. Nikoloas Voros Et Al. "Applied Reconfigurable Computing: Architectures, Tools and Applications" Springer, 2018.
3. Koen Bertels, João M.P. Cardoso, Stamatis Vassiliadis, "Reconfigurable Computing: Architectures and Applications", Springer 2006.

Journals:

1. Mansureh, M.S., Cho, JM., Choi, K. (2016). Reconfigurable Architectures. In: Ha, S., Teich, J. (eds) Handbook of Hardware/Software Codesign. Springer, Dordrecht. https://doi.org/10.1007/97809400170735804_1201

Video Reference:

1. https://www.youtube.com/watch?v=o5hhEJrHH4c
2. https://www.youtube.com/watch?v=5_H_j72Ftq8

NPTEL Courses:

1. https://archive.nptel.ac.in/courses/106/106/106106088/
2. https://www.coursera.org/learn/fpga-intro

4. Course Outcomes

CO. No.	Course Outcome
P23VL512.1	Understand the different architectural principles relevant to reconfigurable computing systems
P23VL512.2	Compare the tradeoffs that are necessary to meet the area, power, and timing criteria of reconfigurable systems
P23VL512.3	Analyze the algorithms related to placement and partitioning
P23VL512.4	Analyze the communication techniques and system on programmable chips for reconfigurable architectures
P23VL512.5	Apply the principles of Network and System on a Programmable Chip

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Program Elective IV

Sl. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
THEORY								
1	P23VL513	Hardware Architectures for Artificial Intelligence and Machine Learning	PE	3	3	0	0	3
2	P23VL514	System-on-Chip Design	PE	3	3	0	0	3
3	P23VL515	Networks on Chip	PE	3	3	0	0	3
4	P23VL516	Design and Analysis of Computer Algorithms	PE	3	3	0	0	3

P23VL513	HARDWARE ARCHITECTURES FOR ARTIFICIAL INTELLIGENCE AND MACHINE LEARNING	L	T	P	C
		3	0	0	3

1. Course Description

The course provides students with a comprehensive understanding of the hardware aspects of AI and machine learning systems, equipping them with the knowledge and skills to design, optimize, and deploy efficient hardware architectures for cutting-edge AI applications.

2. Course Objectives:

1. To introduce new paradigms in computing.
2. To familiarize various aspects and issues in the implementation of machine learning systems
3. To impart background on the application of FPGAs and unconventional computing platforms for machine learning.
4. To provide exposure to using state-of-the-art computing tools.

3. Syllabus

Unit-I: Introduction to Machine Learning Algorithms

Machine learning -Examples of Machine Learning applications-Learning Associations-Classification-Regression-Unsupervised Learning-Reinforcement Learning-Supervised learning: Learning a class from Examples-Regression-Model Selection and Generalization.

Unit-II: Computing Platforms and Processors

Computing Platforms for Machine Learning - Processors - GPU and GPGPUs– FPGA Platforms - SBC Platforms

Unit-III: Cloud Hadoop and IoT

Introduction to Hadoop-Hadoop Architecture-Hadoop Distributed File System-Introduction to IoT - IoT Architecture-IoT Enabling Technologies - IoT Services and Applications

Unit-IV: Neural Networks

Custom Architectures - Neural Network Architectures - Spike Neural Networks – Cellular Neural Network - Generational Adversarial Networks (Gans) - Quality Metrics and Implementation Issues.

Unit-V: Digital Technologies and Cyber Physical Systems

Case Studies in Digital Technologies and Cyber Physical Systems - Security for IoT and Cloud - Assurance of Integrity - Security and Confidentiality.

Text Books:

1. Ethem Alpaydin, "Introduction to Machine Learning", The MIT Press, 2020
2. Mitchell, Tom, "Machine Learning", New York, McGraw-Hill, First Edition, 2017

References:

Reference Books:

1. David B. Kirk, Wen-Mei W. Hwu, Programming Massively Parallel Processors: A Hands-on Approach, Second Edition, Morgan Kauffman, 2016.

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2. Bertil Schmidt, Bioinformatics: High Performance Parallel Computer Architectures, CRC Press, 2011.

Journals:

1. Efficient Hardware Architectures for Accelerating Deep Neural Networks: Survey, International Journal of Artificial Intelligence and Applications (IJAIA), IEEE Access Vol.9, No.1, January 2018.
2. Hardware Design for Machine Learning, International Journal of Artificial Intelligence and Applications (IJAIA), Vol.9, No.1, January 2018.

Video Reference:

1. https://www.youtube.com/watch?v=ukzFI9rgwfU
2. https://www.youtube.com/watch?v=VVg1YBosu5E

NPTEL Courses:

1. https://onlinecourses.nptel.ac.in/noc23_cs18/preview
2. https://onlinecourses.nptel.ac.in/noc22_me44/preview

4. Course Outcomes

CO. No.	Course Outcome
P23VL513.1	Understand Machine learning and its concepts
P23VL513.2	Understand high-performance machine learning architectures.
P23VL513.3	Apply computing paradigms for machine intelligence problems.
P23VL513.4	Analyze solutions and platforms for dataflow-intensive problems.
P23VL513.5	Apply the use of diverse technologies to design efficient applications.

P23VL514	SYSTEM-ON-CHIP DESIGN	L	T	P	C
		3	0	0	3

1. Course Description

System on Chip (SoC) design is the process of integrating all the components required for a complete electronic system into a single chip. SoCs typically include a combination of digital, analog, and mixed-signal components such as processors, memory, input/output interfaces, and specialized hardware accelerators. The benefits of SoCs, such as increased performance, reduced power consumption, and smaller form factors, make them an attractive option for a wide range of applications, from consumer electronics to automotive and industrial applications.

2. Course Objectives

1. To introduce design, optimization, and programming a modern System-on-a-Chip.
2. To detail SoC design with on-chip memories and communication networks, I/O interfacing.
3. To make them understand about signal integrity aware SoC design and scheduling algorithms.
4. To study various bus architectures such as AMBA and Core Connect, and explore processor customization approaches
5. To explore hardware-software co-design, task partitioning, and the use of soft and hard processors in FPGA-based systems.

3. Syllabus

Unit-I: System Architecture Overview

Components of the system – Processor architectures – Memory and addressing – system-level interconnection – SoC design requirements and specifications – design integration – design complexity – cycle time, die area and cost, ideal and practical scaling, the area-time-power tradeoff in processor design, configurability

Unit-II: Processor Selection for SOC

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Overview – soft processors, processor core selection. Basic concepts – instruction set, branches, interrupts and exceptions. Basic elements in instruction handling – Minimizing pipeline delays – reducing the cost of branches – Robust processors – Vector processors, VLIW processors, Superscalar processors
Unit-III: Memory Design
SoC external memory, SoC internal memory, Scratchpads and cache memory – cache organization and write policies – strategies for line replacement at miss time – split I- and D-caches – multilevel caches – SoC memory systems – board-based memory systems – simple processor/memory interaction
Unit-IV: Interconnect Architectures and SOC Customization
Bus architectures – SoC standard buses – AMBA, Core Connect – Processor customization approaches – Reconfigurable technologies – mapping designs onto reconfigurable devices – FPGA-based design – Architecture of FPGA, FPGA interconnect technology, FPGA memory, Floor plan and routing
Unit-V: FPGA-Based Embedded Processor
Hardware-software task partitioning – FPGA fabric Immersed Processors – Soft Processors and Hard Processors – Tool flow for Hardware/Software Co-design –Interfacing Processor with memory and peripherals – Types of On-chip interfaces – Wishbone interface, Avalon Switch 51 Matrix, OPB Bus Interface, Creating a Customized Microcontroller - FPGA-based Signal Interfacing and Conditioning
Text Books:
1. Michael J Flynn and Wayne Luk, "Computer system Design: System-on-Chip", Wiley-India, 2012. 2. J. Bhasker, Rakesh Chadha, STA for Nanometer design – A practical approach, Springer, First Edition, 2010.
References:
Reference Books 1. Laung-Terng Wang, Charles E. Stroud, Nur A. Touba, System-on-Chip Test Architectures: Nanometer Design for Testability, Morgan Kaufmann, First Edition, 200-. 2. Ahmed Jerraya and Wayne Wolf, Multiprocessor Systems-on-Chips (Systems on Silicon Series), Morgan Kaufmann, First Edition, 2010. **Journals:** 1. System-on-Chip (SoC) Design and Its Applications 2. Design and Optimization of System-on-chip (SOC) **Video Reference:** 1. https://www.youtube.com/watch?v=PRQXzjTrCJY 2. https://www.youtube.com/watch?v=X4z1U8dJCTc **NPTEL Courses:** 1. https://www.udemy.com/topic/soc/ 2. https://nanohub.org/courses/ECE695R/o1a

4. Course Outcomes

CO. No.	Course Outcome
P23VL514.1	Explain all important components of a System-on-Chip and an embedded system
P23VL514.2	Design the digital hardware and embedded software
P23VL514.3	Outline the major design flows for digital hardware and embedded software
P23VL514.4	Discuss the major architectures and trade-offs concerning performance, cost, & power
P23VL514.5	Understand the single chip and embedded systems in SOC Design

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5P23VL515	NETWORKS ON CHIP	L	T	P	C
		3	0	0	3

1. Course Description

Networks on Chip (NoCs) are a type of communication architecture that interconnects various components within a single integrated circuit (IC) or system-on-chip (SoC). They are designed to facilitate the communication between multiple processing elements, memory modules, and other IP blocks on a chip. NoCs use various routing algorithms to efficiently deliver data packets from the source to the destination. This includes deterministic routing, adaptive routing, and hybrid routing approaches. NoC provide a scalable and efficient communication infrastructure for complex SoCs, enabling high-performance and energy-efficient computing systems.

2. Course Objectives:

1. NoCs aim to provide high-performance communication between cores or processing Elements
2. NoCs are designed to scale efficiently with increasing numbers of cores
3. NoCs are designed to be power-efficient, using techniques such as clock gating, power gating
4. NoCs are designed to be easy to design and verify, with tools and methodologies
5. NoCs can incorporate features for reliable communication

3. Syllabus

Unit-I: Introduction to NoC

Introduction to NOC – OSI Layer Rules in NOC - Interconnection Networks in Network-On-Chip Network Topologies - Switching Techniques - Routing Strategies - Flow Control Protocol Quality of-Service Support.

Unit-II: Architecture Design

Switching Techniques and Packet Format - Asynchronous FIFO Design - GALS Style of Communication - Wormhole Router Architecture Design - VC Router Architecture Design - Adaptive Router Architecture Design.

Unit-III: Routing Algorithm

Packet Routing-QOS, Congestion Control and Flow Control – Router Design – Network Link Design – Efficient and Deadlock-Free Tree-Based Multicast Routing Methods - Path-Based Multicast Routing For 2D and 3D Mesh Networks- Fault-Tolerant Routing Algorithms - Reliable and Adaptive Routing Algorithms.

Unit-IV: Test and Fault Tolerance of NoC

Design-Security in Networks-On-Chips-Formal Verification of Communications in Networks-On Chips-Test and Fault Tolerance for Networks-On-Chip Infrastructures-Monitoring Services for Networks-On-Chips.

Unit-V: Three-Dimensional Integration of Network-On-Chip

Three-Dimensional Networks-On-Chips Architectures – A Novel Dimensionally-Decomposed Router for On-Chip Communication in 3D Architectures - Resource Allocation for QOS On-Chip Communication – Networks-On-Chip Protocols-On-Chip Processor Traffic Modeling for Networks On-Chip.

Text Books:

1. Chrysostomos Nicopoulos, Vijaykrishnan Narayanan, Chita R.Das" Networks-On - Chip " Architectures Holistic Design Exploration", Springer 2010
2. Konstantinos Tatas and Kostas Siozios "Designing 2D and 3D Network-On-Chip Architectures" Springer, 2013

References:

Reference Books

1. Fayezgebali, Haythamelmiligi, Hqhahedwatheq E1-Kharashi "Networks-On-Chips Theory and Practice CRC Press, 2009

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2. Palesi, Maurizio, Daneshtalab, Masoud "Routing Algorithms in Networks-On-Chip" Springer, 2014

Journals:

1. Network-on-Chip: The Next Generation of System-on-Chip Integration (DOI:10.1201/978131521602)
2. Networks-On-Chip (https://link.springer.com/book/10.1007/b105353)

Video Reference:

1. https://www.youtube.com/watch?v=7-KJ3BnFsr8
2. https://www.youtube.com/watch?v=6X4R-jkdyYE

NPTEL Courses:

1. https://archive.nptel.ac.in/courses/106/103/106103183/
2. https://archive.nptel.ac.in/noc/courses/noc21/SEM2/noc210cs95/

4. Course Outcomes

CO. No.	Course Outcome
P23VL515.1	Compare different architecture design
P23VL515.2	Discuss different routing algorithms
P23VL515.3	Explain three dimensional Networks on Chip architectures
P23VL515.4	Test and design fault tolerant NOC
P23VL515.5	Design three dimensional architectures of NOC

P23VL516	Design and Analysis of Computer Algorithms	L	T	P	C
		3	0	0	3

1. Course Description

The primary objective of this course is to introduce the concept of algorithm as a precise mathematical concept, and study how to design algorithms, establish their correctness, study their efficiency and memory needs. The course consists of a strong mathematical component in addition to the design of various algorithms.

2. Course Objectives:

1. To demonstrate performance of algorithms with respect to time and space complexity.
2. To explain graph and tree traversals.
3. To explain the concepts greedy method and dynamic programming. Applying for several applications like knapsack problem, job sequencing with deadlines, and optimal binary search tree, TSP and so on respectively.
4. To Illustrate the methods of backtracking and branch bound techniques to solve the problems like n-queens' problem, graph colouring and TSP respectively.
5. To familiarize the concepts of deterministic and non-deterministic algorithms.

3. Syllabus

Unit-I: Introduction

Algorithm, pseudo code for expressing algorithms, performance analysis-space complexity, time complexity, asymptotic notation- big (O) notation, omega notation, theta notation and little (o) notation, recurrences, probabilistic analysis, disjoint set operations, union and find algorithms.

Unit-II: Divide & Conquer and Greedy Method

DIVIDE AND CONQUER: General method, applications-analysis of binary search, quick sort, merge sort, AND OR Graphs.

GREEDY METHOD: General method, Applications-job sequencing with deadlines, Fractional knapsack problem, minimum cost spanning trees, Single source shortest path problem.

Unit-III: Graphs and Dynamic Programming

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GRAPHS (Algorithm and Analysis): Breadth first search and traversal, Depth first search and traversal, Spanning trees, connected components and bi-connected components, Articulation points.
DYNAMIC PROGRAMMING: General method, applications - optimal binary search trees, 0/1 knapsack problem, All pairs shortest path problem, Travelling sales person problem, Reliability design.

Unit-IV: Backtracking, Branch and Bound

BACKTRACKING: General method, Applications- n-queen problem, Sum of subsets problem, Graph coloring and Hamiltonian cycles.
BRANCH AND BOUND: General method, applications - travelling sales person problem, 0/1 knapsack problem- LC branch and bound solution, FIFO branch and bound solution.

Unit-V: NP-Hard and NP-Complete Problems

Basic concepts, non-deterministic algorithms, NP-hard and NP-complete classes, Cook's theorem.

Text Books:

1. Ellis Horowitz, Satraj Sahni, Rajasekharam (2020), Fundamentals of Computer Algorithms, 2nd edition, University Press, New Delhi.
2. Aho, Ullman, Hopcroft (2009), Design and Analysis of algorithms, 2nd edition, Pearson education, New Delhi

References:

Reference Books

1. R. C. T. Lee, S. S. Tseng, R.C. Chang and T. Tsai (2006), Introduction to Design and Analysis of Algorithms A strategic approach, McGraw Hill, India.
2. Allen Weiss (2009), Data structures and Algorithm Analysis in C++, 2nd edition, Pearson education, New Delhi.

Journals:

1. International Journal of Algorithms Design and Analysis Review

Video Reference:

1. https://www.youtube.com/watch?v=d4Rxzaofesl
2. https://www.slideserve.com/efia/design-and-analysis-of-algorithms

NPTEL Courses:

1. https://onlinecourses.nptel.ac.in/noc19_cs47/preview

4. Course Outcomes

CO. No.	Course Outcome
P23VL516.1	Identify various Time and Space complexities of various algorithms
P23VL516.2	Understand Tree Traversal method and Greedy Algorithms
P23VL516.3	Apply Dynamic Programming concept to solve various problems
P23VL516.4	Apply Backtracking, Branch and Bound concept to solve various problems
P23VL516.5	Implement different performance analysis methods for non-deterministic algorithms

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Semester III

Sl. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
THEORY								
1	P23VL5XX	Program Elective V	PE	3	3	0	0	3
2	P23VL5XX	Program Elective VI	PE	3	3	0	0	3
3	P23OXXXX	Open Elective	OE	3	3	0	0	3
PRACTICALS								
4	P23VL601	Project Work Phase I	PW	16	0	0	16	8
		TOTAL		**25**	**9**	**0**	**16**	**17**

Program Elective V

Sl. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
THEORY								
1	P23VL517	Semiconductor Memory Design	PE	3	3	0	0	3
2	P23VL518	Signal Integrity for High-Speed Design	PE	3	3	0	0	3
3	P23VL519	Nanoscale Devices	PE	3	3	0	0	3
4	P23VL520	MEMS and NEMS	PE	3	3	0	0	3

P23VL517	SEMICONDUCTOR MEMORY DESIGN	L	T	P	C
		3	0	0	3

1. Course Description

Modern digital systems require the capability of storing and retrieving large amounts of information at high speeds. Memories are circuits or systems that store digital information in large quantity. The analysis and design of VLSI memories, commonly known as semiconductor memories. Today, memory circuits come in different forms including SRAM, DRAM, ROM, EPROM, E2PROM, Flash, and FRAM. While each form has a different cell design, the basic structure, organization, and access mechanisms are largely the same.

2. Course Objectives:

1. To understand the architectures and applications of SRAM memories
2. To understand the architectures and applications of DRAM memories
3. To learn the different Non-Volatile memories.
4. To analyse the reliability and radiation hardening process and issues of the memory design.
5. To learn advanced high-density memory technologies and testing

3. Syllabus

Unit-I: STATIC RANDOM ACCESS MEMORY

Static Random Access Memories (SRAMs): SRAM cell structures-MOS SRAM architecture-MOS SRAM cell and peripheral circuit operation-Bipolar SRAM technologies-Silicon on Insulator (SOI) technology-Advanced SRAM architectures and technologies-Application specific SRAMs.

Unit-II: DYNAMIC RANDOM ACCESS MEMORY

Dynamic Random Access Memories (DRAMs): DRAM technology development-CMOS DRAMs-DRAMs cell theory and advanced cell structures-Bi CMOS, DRAMs-Soft error failures in DRAMs-Advanced DRAM designs and architecture-Application, Specific DRAMs.

Unit-III: NON VOLATILE MEMORIES

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Masked Read-Only Memories (ROMs)-High density ROMs-Programmable Read-Only Memories (PROMs)-Bipolar PROMs-CMOS PROMs-Erasable (UV) - Programmable Road-Only Memories (EPROMs)-Floating-Gate EPROM Cell-One-Time Programmable (OTP) EPROMs-Electrically Erasable PROMs (EEPROMs)-EEPROM Technology And Architecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory Architecture.
Unit-IV: RELIABILITY AND RADIATION EFFECTS
General reliability issues-RAM failure modes and mechanism-Nonvolatile memory reliability-Reliability modeling and failure rate prediction-Design for reliability- Reliability test structures-Reliability screening and qualification. RAM fault modeling- Electrical testing- Pseudo random testing-Megabit DRAM testing- Nonvolatile memory modeling and testing- IDDQ fault modeling and testing-Application specific memory testing.
Unit-V: ADVANCED MEMORY TECHNOLOGIES
High-Density Memory Packaging Technologies, Ferroelectric Random Access Memories (FRAMs)-Analog Memories-Magneto-resistive Random Access Memories (MRAMs)-Experimental Memory Devices Memory Hybrids and MCMs (2D)- Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability.
Text Books:
1. Ashok K. Sharma, "Semiconductor Memories Technology, Testing, and Reliability", Wiley-IEEE Press Publishers, 1st Edition, 2002. 2. Tegze P. Haraszti, "CMOS Memory Circuits", Kluwer Academic Publishers, 2002 Edition, 2007.
References:
Reference Books 1. Roberto Gastaldi and Giovanni Campardo in Search of the Next Memory: Inside the Circuitry from the Oldest to the Emerging Non-Volatile Memories, Springer, 2017. 2. Ashok K. Sharma, "Advanced Semiconductor Memories: Architectures, Designs, and Applications", Wiley- IEEE Press Publishers, 1st Edition, 2003. **Journals:** 1. https://www.sciencedirect.com/journal/microprocessors-and-microsystems 2. https://www.sciencedirect.com/journal/aeu-international-journal-of-electronics-and-communications **Video Reference:** 1. https://www.youtube.com/watch?v=jK6xr4r06tU 2. https://www.youtube.com/watch?v=XbKOmOPjLtc&list=PL5Q2soXY2Zi9gM4xiJpvMEHRsepFCDDP3 **NPTEL Courses:** 1. https://nptel.ac.in/courses/108108122

4. Course Outcomes

CO. No.	Course Outcome
P23VL517.1	Understand the architectures and applications of SRAM memories
P23VL517.2	Understand the architectures and applications of DRAM memories
P23VL517.3	Utilize the different Non-Volatile memories.
P23VL517.4	Analyze the reliability and radiation hardening process and issues of the memory design.
P23VL517.5	Examine advanced high-density memory technologies and testing.

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P23VL518	SIGNAL INTEGRITY FOR HIGH-SPEED DESIGN	L	T	P	C
		3	0	0	3

1. Course Description

This course delves into the essential concepts and techniques of signal integrity in high-speed digital and mixed-signal systems. It addresses the challenges that arise when designing circuits that operate at high frequencies and ensures the reliable transmission of signals without degradation. Students will learn to identify, analyze, and mitigate signal integrity issues, enabling the design of robust high-speed electronic systems.

2. Course Objectives:

1. To understand the principles of signal integrity and its importance in high-speed design.
2. To learn how to model, simulate, and analyze signal integrity issues.
3. To develop strategies for mitigating signal integrity problems in high-speed circuits.
4. To gain hands-on experience with simulation tools and measurement techniques.
5. To examine clock distribution challenges and termination techniques, to optimize clock performance in high-speed digital systems.

3. Syllabus

Unit-I: Signal Propagation on Transmission Lines

Transmission line equations, wave solution, wave vs. circuits, initial wave, delay time, Characteristic impedance , wave propagation, reflection, and bounce diagrams Reactive terminations – L, C , static field maps of micro strip and strip line cross-sections, per unit length parameters, PCB layer stackups and layer/Cu thicknesses, cross-sectional analysis tools, Zo and Td equations for microstrip and stripline Reflection and terminations for logic gates, fan-out,logic switching , input impedance into a transmission-line section, reflection coefficient, skin- effect, dispersion.

Unit-II: Multi-Conductor Transmission Lines and Cross-Talk

Multi-conductor transmission-lines, coupling physics, per unit length parameters ,Near and far- end cross-talk, minimizing cross-talk (stripline and microstrip) Differential signalling, termination, balanced circuits , S-parameters, Lossy and Lossless models.

Unit-III: Non-Ideal Effects

Non-ideal signal return paths – gaps, BGA fields, via transitions, Parasitic inductance and capacitance, Transmission line losses – Rs, tanδ, routing parasitic, Common-mode current, differential-mode current, Connectors.

Unit-IV: Power Considerations and System Design

SSN/SSO, DC power bus design, layer stack up, SMT decoupling, Logic families, power consumption, and system power delivery, Logic families and speed Package types and parasitic ,SPICE, IBIS models ,Bit streams, PRBS and filtering functions of link-path components, Eye diagrams, jitter, inter-symbol interference Bit-error rate ,Timing analysis.

Unit-V: Clock Distribution and Clock Oscillators

Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, cancelling parasitic capacitance, Clock jitter.

Text Books:

1. H. W. Johnson and M. Graham, High-Speed Digital Design: A Handbook of Black Magic, Prentice Hall, January 2003.
2. Douglas Brooks, Signal Integrity Issues and Printed Circuit Board Design, Prentice Hall PTR, November 2012.

References:

Reference Books:

1. S. Hall, G. Hall, and J. McCall, High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices, Wiley-Interscience, January 2014.
2. Eric Bogatin , Signal Integrity – Simplified , Prentice Hall PTR, 3rd Edition, June 2018.

Journals:

1. https://www.signalintegrityjournal.com/keywords/192-high-speed

Video Reference:

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1. https://www.youtube.com/watch?v=oxrXfIimy_Q **NPTEL Courses:** 1. https://nptel.ac.in/courses/108105375

4. Course Outcomes

CO. No.	Course Outcome
P23VL518.1	Identify sources affecting the speed of digital circuits.
P23VL518.2	Recognize methods to improve the signal transmission characteristics
P23VL518.3	Analyze the different non-ideal effects
P23VL518.4	Analyze the system power dissipation
P23VL518.5	Ability to analyze clocking strategies

P23VL519	NANOSCALE DEVICES	L	T	P	C
		3	0	0	3

1. Course Description

The Nanoscale Devices course offers a comprehensive examination of the principles, design, and fabrication of devices at the nanoscale. The course provides an in-depth exploration of the fundamental principles of nanotechnology and its practical use in electronic devices. The course provides an in-depth understanding of the fundamental principles of nanotechnology and their practical use in electronic devices. Students will learn the fundamental physical principles that control materials and devices at the nanoscale. They will also study the methods employed to manufacture these devices and explore their applications across many fields. This course will introduce the fundamental principles of physics as applied to innovative, small-scale, mesoscopic and nanoscopic technologies.

2. Course Objectives:

1. To understand the basic principles of nanotechnology and nanoscale device operation.
2. To apply quantum mechanical concepts to the analysis of nanoscale devices.
3. To identify and utilize various materials and fabrication techniques for creating nanoscale devices.
4. To characterize nanoscale materials and devices using advanced microscopy and spectroscopy techniques.
5. To analyze the performance and potential applications of various nanoscale devices.

3. Syllabus

Unit-I: INTRODUCTION TO NOVEL MOSFETS

MOSFET scaling, short channel effects - channel engineering - source/drain engineering - high k dielectric - copper interconnects - strain engineering, SOI MOSFET, multigate transistors – single gate – double gate – triple gate – surround gate, quantum effects – volume inversion – mobility – threshold voltage – inter subband scattering, multigate technology – mobility – gate stack

Unit-II: PHYSICS OF MULTIGATE MOS SYSTEMS

MOS Electrostatics – 1D – 2D MOS Electrostatics, MOSFET Current-Voltage Characteristics – CMOS Technology – Ultimate limits, double gate MOS system – gate voltage effect - semiconductor thickness effect – asymmetry effect – oxide thickness effect – electron tunnel current – two-dimensional confinement, scattering – mobility

Unit-III: NANOWIRE FETS AND TRANSISTORS AT THE MOLECULAR SCALE

Silicon nanowire MOSFETs – Evaluvation of I-V characteristics – The I-V characteristics for non-degenerate carrier statistics – The I-V characteristics for degenerate carrier statistics – Carbon nanotube

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– Band structure of carbon nanotube – Band structure of graphene – Physical structure of nanotube – Band structure of nanotube – Carbon nanotube FETs – Carbon nanotube MOSFETs
Unit-IV: RADIATION EFFECTS
Radiation effects in SOI MOSFETs, total ionizing dose effects – single gate SOI – multigate devices, single event effect, scaling effects.
Unit-V: CIRCUIT DESIGN USING MULTIGATE DEVICES
Digital circuits – impact of device performance on digital circuits – leakage performance trade off – multi-VT devices and circuits – SRAM design, analog circuit design – transconductance - intrinsic gain – flicker noise – self heating –band gap voltage reference – operational amplifier – comparator designs, mixed signal – successive approximation DAC, RF circuits.
Text Books:
1. Khurshed Ahmad Shah, Farooq Ahmad Khanday. "Nanoscale Electronic Devices and Their Applications" CRC Press, 2023 2. Mark Lundstrom, Jing Guo, "Nanoscale Transistors: Device Physics, Modeling and Simulation", Springer, 2006
References:
Reference Books 1. J P Colinge, "FINFETs and other multi-gate transistors", Springer – Series on integrated circuits and systems, 2008 2. M S Lundstorm, "Fundamentals of Carrier Transport", 2nd Ed., Cambridge University Press, Cambridge UK, 2000 **Journals:** 1. https://www.nature.com/subjects/nanoscale-devices 2. https://www.rsc.org/journals-books-databases/about-journals/nanoscale/ **Video Reference:** 1. https://www.youtube.com/playlist?list=PLLy_2iUCG87AUZ9mkKZT7fu3HFispgKve **NPTEL Courses:** 1. https://archive.nptel.ac.in/noc/courses/noc22/SEM1/noc22-ee47/

4. Course Outcomes

CO. No.	Course Outcome
P23VL519.1	Interpret novel MOSFET devices and understand the advantages of multi-gate devices
P23VL519.2	Discuss the physical insight of their functional characteristics
P23VL519.3	Interpret Nanowire FETs and transistors at the molecular scale
P23VL519.4	Analyze the effects of radiation in nanoscale devices and its applications
P23VL519.5	Understand and develop various types of nanoscale memory devices

P23VL520	MEMS AND NEMS	L	T	P	C
		3	0	0	3

1. Course Description

The course is introduced to learn about micro- and nano-scale devices. After completing this course, students will have an idea about MEMS and NEMS devices and their applications. They will know how to design, analyze and characterize a micro or nano system. They will also have an idea about MEMS fabrication.

2. Course Objectives:

1. To define and explain the fundamental principles and characteristics of Micro-Electro-Mechanical Systems (MEMS) and Nano-Electro-Mechanical Systems (NEMS)
2. To identify and describe various applications of MEMS and NEMS devices

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3. To design, analyze, and characterize micro- and nano-scale systems 4. To understand the fabrication process of MEMS devices 5. To apply their knowledge to develop innovative solutions using MEMS and NEMS technology
3. Syllabus
Unit-I: INTRODUCTION TO MEMS and NEMS
Overview of micro and Nano technologies - Miniaturization significance and advantages -Micro electro mechanical systems and Nano Electro mechanical systems, devices and technologies, Laws of scaling - Survey of materials - Smart Sensors - Applications of MEMS and NEMS.
Unit-II: MICRO-MACHINING AND MICROFABRICATION TECHNIQUES
Photolithography - material Synthesis techniques - Film deposition - Etching Processes- wafer bonding - Bulk micro machining, silicon surface micro machining - LIGA process.
Unit-III: MICRO SENSORS AND MICRO ACTUATORS
Transduction mechanisms in different energy domain-Micromachined capacitive, Piezoelectric, piezoresistive and Electromechanical and thermal sensors/actuators and applications
Unit-IV: NANOELECTRONICS DEVICES AND NEMS TECHNOLOGY
Nano electronics devices and applications – SET– RTD – Memristor – QCA - molecular Electronics - Nano Fabrication techniques - atomic scale precision Engineering- NEMS in measurement, sensing, actuation and systems design.
Unit-V: MEMS AND NEMS APPLICATION
Micro/Nano Fluids and applications- Bio MEMS- Optical NEMS- Micro and Nano motors-Quantum computing.
Text Books:
1. Chang Liu, "Foundations of MEMS", Pearson International Edition, 2006 2. Marc F madou "Fundamentals of micro fabrication" CRC Press 2002 2nd Edition. 3. M.H.Bao "Micromechanical transducers :Pressure sensors, accelerometers and gyroscopes", Elsevier, Newyork, 2000.
References:
Reference Books 1. Mohamed Gad - el - Hak "MEMS Handbook" Edited CRC Press 2002 2. Sabriesolomon "Sensors Handbook", Mc Graw Hill 1998. 2. Tai-Ran Hsu, "MEMS and Microsystems: design, manufacture, and Nanoscale"- 2nd Edition, John Wiley & Sons, Inc., Hoboken, New Jersey, 2008 3. Lyshevski, S.E. "Nano- and Micro-Electromechanical Systems: Fundamentals of Nano-and Microengineering "(2nd ed.). CRC Press,2005. **Journals:** 1. https://link.springer.com/referenceworkentry/10.1007/978-0-387-30877-7_9 2. https://www.sciencedirect.com/science/article/abs/pii/S0079681613000178 **Video Reference:** 1. https://www.youtube.com/watch?v=j9y0gfN9WMg&list=PL5873EDBDFB69BAD8 2. https://www.youtube.com/watch?v=8CdVb6z3ViM 3. https://www.youtube.com/watch?v=CjFXlkAeYH0 **NPTEL Course:** 1. https://nptel.ac.in/courses/108106165

4. Course Outcomes

CO. No.	Course Outcome
P23VL520.1	Explain the material properties and the significance of MEMS and NEMS for industrial automation.
P23VL520.2	Demonstrate knowledge delivery on micromachining and micro fabrication.
P23VL520.3	Apply the fabrication mechanism for MEMS sensor and actuators.
P23VL520.4	Apply the concepts of Nano electronics and NEMS to models, simulate and process the sensors and actuators.
P23VL520.5	Improved Employability and entrepreneurship capacity due to knowledge up gradation on MEMS and NEMS technology.

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Program Elective VI

Sl. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
THEORY								
1	P23VL521	RF IC Design	PE	3	3	0	0	3
2	P23VL522	Hardware Security	PE	3	3	0	0	3
3	P23VL523	Electronic Packaging Technologies	PE	3	3	0	0	3
4	P23VL524	Advanced Computer Architecture and Parallel Processing	PE	3	3	0	0	3

P23VL521	RF IC DESIGN	L	T	P	C
		3	0	0	3

1. Course Description

This course provides an in-depth study of the design and analysis of radio frequency integrated circuits (RF ICs). It covers the fundamental concepts, design techniques, and practical considerations required to create high-performance RF circuits. The course bridges the gap between theoretical understanding and real-world applications, equipping students with the skills needed to tackle complex RF design challenges.

2. Course Objectives:

1. To understand the fundamental principles of RF circuit design.
2. To learn the techniques for designing, analyzing, and testing RF ICs.
3. To gain practical experience in using RF design tools and simulation software.
4. To develop the ability to solve complex design problems and optimize RF circuits for performance and reliability.

3. Syllabus

Unit-I: CMOS Physics, Transceiver Specifications and Architectures

Introduction to MOSFET Physics, Noise: Thermal, shot, flicker, popcorn noise, Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link, Homodyne Receiver, Heterodyne Receiver, Image reject, Low IF Receiver Architectures Direct up-conversion Transmitter, Two step up-conversion Transmitter.

Unit-II: Impedance Matching and Amplifiers

S-parameters with Smith chart, Passive IC components, Impedance matching networks, Common Gate, Common Source Amplifiers, OC Time constants in bandwidth estimation and enhancement, High frequency amplifier design, Power match and Noise match, Single ended and Differential LNAs, Terminated with Resistors and Source Degeneration LNAs.

Unit-III: Feedback Systems and Power Amplifier

Stability of feedback systems: Gain and phase margin, Root-locus techniques, Time and Frequency domain considerations, Compensation, General model – Class A, AB, B, C, D, E and F amplifiers, Power amplifier Linearization Techniques, Efficiency boosting techniques, ACPR metric, Design considerations

Unit-IV: Mixers and Oscillator

Mixer characteristics, Non-linear based mixers, Quadratic mixers, Multiplier based mixers, Single balanced and double balanced mixers, subsampling mixers, Oscillators describing Functions, Colpitts oscillators Resonators, Tuned Oscillators, Negative resistance oscillators, Phase noise.

Unit-V: PLL and Frequency Synthesizers

Linearized Model, Noise properties, Phase detectors, Loop filters and Charge pumps, Integer-N frequency synthesizers, Direct Digital Frequency synthesizers.

Text Books:

1. T.Lee, "Design of CMOS RF Integrated Circuits", Cambridge, 2004.

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2. B.Razavi, "RF Microelectronics", Pearson Education, 2nd Edition, January 2013.

References:

Reference Books:

1. Jan Crols, Michiel Steyaert, "CMOS Wireless Transceiver Design", Kluwer Academic Publishers, January 2015.
2. B.Razavi, "Design of Analog CMOS Integrated Circuits", McGraw Hill, 2 nd Edition, November 2017.

Journals:

1. https://ieee-cas.org/publication/ieee-rfic-virtual-journal
2. https://rfic-ieee.org/

Video Reference:

1. https://www.youtube.com/watch?v=KUDGGsyh1Hs

NPTEL Courses:

1. https://archive.nptel.ac.in/courses/117/102/117102012/

4. Course Outcomes

CO. No.	Course Outcome	BTL	POs	PSOs
P23VL521.1	Understand the user specifications for RF systems	K2	1,3,4,5, 6	-
P23VL521.2	Apply the impedance matching concepts in RF amplifiers	K3	1,3,4,5, 6	-
P23VL521.3	Ability to analyze and design RF power amplifiers	K4	1,3,4,5, 6	-
P23VL521.4	Analyze and design RF mixers and oscillators	K4	1,3,4,5, 6	-
P23VL521.5	Analyze and design PLL for RF based applications	K4	1,3,4,5, 6	-

P23VL522	HARDWARE SECURITY	L	T	P	C
		3	0	0	3

1. Course Description

This course provides a comprehensive overview of VLSI design with a focus on hardware security, introduction to the principles of hardware security, focusing on securing embedded systems and hardware components in engineering applications also deals with threats to hardware, countermeasures, secure design practices, and case studies relevant to electronics engineering.

2. Course Objectives:

1. To provide a solid understanding of fundamental concepts in VLSI design and hardware security.
2. To identify and analyze various security threats and vulnerabilities specific to VLSI systems.
3. To apply security-enhancing techniques, such as hardware obfuscation, PUFs, and tamper detection, in VLSI designs.
4. To evaluate the effectiveness of various hardware security mechanisms and protocols.
5. To Explore Emerging Topics in Hardware Security.

3. Syllabus

Unit-I: Introduction to Hardware Security

Overview of hardware security- Importance of hardware security in electronics engineering-Types of hardware attacks: side-channel attacks, fault injection. Cryptographic Primitives for Hardware Security: Symmetric and asymmetric encryption, Crptographic algorithms and their implementation in hardware, Hardware-based random number generation.

Unit-II: Hardware Vulnerabilities

Introduction to Hardware vulnerabilities: Physical attacks like probing, micro probing, Reverse engineering and tampering, Case studies of hardware vulnerabilities in electronic systems. Secure Hardware Design Principles: Secure boot and trusted execution environments, Design for testability and security, Hardware obfuscation and logic locking.

Unit-III: Embedded System Security

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Overview of Embedded system security: Security in microcontrollers and FPGAs, Secure communication protocols, Authentication and access control mechanisms. Hardware Security Fundamentals-Threats to hardware security- Security metrics and evaluation.
Unit-IV: Secure VLSI Design Techniques
Overview of Secure VLSI Design Techniques: boot and trusted execution environments, Hardware obfuscation and logic locking, Design for testability (DFT) and security.
Unit-V: Cryptographic Hardware Design
Implementing cryptographic algorithms in VLSI-Random number generation in hardware Secure key storage and management, Case Studies and Applications in Engineering: Security in automotive electronics and control systems, Industrial control systems and IoT devices.
Text Books:
1. Neil Weste and David Harris , "CMOS VLSI Design: A Circuits and Systems Perspective" Pearson Education India, 2015. 2. Mohammad Tehranipoor and Cliff Wang , "Introduction to Hardware Security and Trust", Springer 2011.
References:
Reference Books 1. Debdeep Mukhopadhyay and Rajat Subhra Chakraborty, "Hardware Security: Design, Threats, and Safeguards" CRC Press,2014. **Journals:** 1. https://link.springer.com/journal/41635/volumes-and-issues 2. https://www.mdpi.com/journal/cryptography/special_issues/Hardware_Security_2022 **Video Reference:** 1. https://www.youtube.com/watch?v=a5tIhkXPi4g **NPTEL Courses:** 1. https://onlinecourses.nptel.ac.in/noc22_cs48/preview

4. Course Outcomes

CO. No.	Course Outcome
P23VL522.1	Understand the fundamental concepts of hardware security.
P23VL522.2	Identify and mitigate hardware security vulnerabilities in VLSI circuits.
P23VL522.3	Apply secure design techniques to develop robust VLSI systems.
P23VL522.4	Apply hardware security measures in engineering contexts.
P23VL522.5	Apply real-world case studies of secure in VLSI applications.

P23VL523	ELECTRONIC PACKAGING TECHNOLOGIES	L	T	P	C
		3	0	0	3

1. Course Description

Electronic Packaging Technologies is a critical component of VLSI design and manufacturing, focusing on the techniques, materials, and challenges in packaging integrated circuits (ICs) for various applications. This course aims to equip students with essential knowledge to understand, design, and implement effective electronic packaging solutions.

2. Course Objectives

1. To understand the principles and importance of electronic packaging in VLSI technology.
2. To gain the ability to analyse different types of electronic packaging technologies and their applications.
3. To design and simulate electronic packages considering thermal, electrical, and mechanical constraints.
4. To gain knowledge of reliability metrics, failure mechanisms, and models in electronic packaging
5. To apply advanced packaging techniques to enhance system performance and functionality.

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3. Syllabus

Unit-I: Introduction to Electronic Packaging

Importance of packaging in VLSI design-Overview of packaging trends and challenges-Fundamentals of Electronic Packaging: Packaging hierarchy: chip, package, board, system -Packaging materials and selection criteria.

Unit-II: Types of Electronic Packaging Technologies

Integrated Circuit (IC) Packaging : BGA, QFN, CSP, and Flip-chip packaging - Wire bonding vs. flip-chip technologies -System-in-Package (SiP) and 3D Packaging : Overview and advantages - Case studies on SiP applications

Unit-III: Thermal Management in Electronic Packaging

Heat Generation and Dissipation: Thermal challenges in VLSI circuits-Thermal management techniques: heat sinks, thermal interface materials -Thermal Simulation and Analysis: Finite Element Analysis (FEA) for thermal modelling - Simulation tools and case studies.

Unit-IV: Reliability and Testing

Reliability Metrics and Standards: Reliability predictions and models -Failure mechanisms in electronic packaging-Testing and Quality Assurance : Accelerated testing methods-Quality control in packaging manufacturing

Unit-V: Advanced Packaging Techniques

Emerging Trends in Electronic Packaging: Organic and inorganic substrates-Additive manufacturing (3D printing) in packaging- Design for Manufacturability (DfM):Design considerations for high-volume manufacturing-Case study: Designing for reliability and manufacturability

Text Books:

1. Charles A. Harper, "Electronic Packaging and Interconnection Handbook", McGraw-Hill Inc 1991.
2. Rao Tummala et al, "Fundamentals of Microelectronics Packaging", McGraw Hill 2001.

Reference Books

1. Bernard S. Matisoff , "Handbook of Electronic Packaging Design and Engineering" Springer 2012.
2. John H. Lau, "3D IC Integration and Packaging", McGraw Hill 2015.

Journals:

1. https://ieeexplore.ieee.org/xpl/RecentIssue.jsp?punumber=5503870
2. https://journaltool.asme.org/home/JournalDescriptions.cfm?JournalID=5#

Video Reference:

1. https://www.youtube.com/watch?v=-egYoxajTz0
2. https://www.youtube.com/watch?v=7gg2eVVayA4

NPTEL Courses:

1. https://archive.nptel.ac.in/courses/108/108/108108031/#

4. Course Outcomes

CO. No.	Course Outcome
P23VL523.1	Understand the fundamental principles of electronics packaging
P23VL523.2	Analyze different types of electronic packages and their applications
P23VL523.3	Analyze materials and manufacturing processes used in electronics packaging
P23VL523.4	Apply reliability engineering principles to assess and improve electronic package reliability
P23VL523.5	Design and optimize electronic packages considering performance, reliability, and manufacturability constraints.

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P23VL524	ADVANCED COMPUTER ARCHITECTURE AND PARALLEL PROCESSING	L	T	P	C
		3	0	0	3

1. Course Description

This course provides an in-depth exploration of advanced topics in computer architecture and parallel processing, focusing on the design, analysis, and optimization of high-performance computing systems. It is designed for students with a solid foundation in computer architecture and programming who wish to delve into the complexities of modern computing systems.

2. Course Objectives:

1. To introduce the recent trends in the field of Computer Architecture and identify performance related parameters.
2. To learn the different multiprocessor issues.
3. To expose the different types of multicore architectures.
4. To understand the design of the memory hierarchy.
5. To explore techniques for detecting and enhancing loop-level parallelism to optimize computing performance.

3. Syllabus

Unit-I: FUNDAMENTALS OF COMPUTER DESIGN AND ILP

Fundamentals of Computer Design – Measuring and Reporting Performance – Instruction Level Parallelism and its Exploitation – Concepts and Challenges –Exposing ILP - Advanced Branch Prediction - Dynamic Scheduling - Hardware-Based Speculation - Exploiting ILP - Instruction Delivery and Speculation - Limitations of ILP - Multithreading

Unit-II: MEMORY HIERARCHY DESIGN

Introduction – Optimizations of Cache Performance – Memory Technology and Optimizations – Protection: Virtual Memory and Virtual Machines – Design of Memory Hierarchies – Case Studies

Unit-III: MULTIPROCESSOR ISSUES

Introduction- Centralized, Symmetric and Distributed Shared Memory Architectures –Cache Coherence Issues – Performance Issues – Synchronization – Models of Memory Consistency – Case Study- Interconnection Networks – Buses, Crossbar and Multi-stage Interconnection Networks

Unit-IV: MULTICORE ARCHITECTURES

Homogeneous and Heterogeneous Multi-core Architectures – Intel Multicore Architectures – SUN CMP architecture – IBM Cell Architecture. Introduction to Warehouse-scale computers Architectures- Physical Infrastructure and Costs- Cloud Computing –Case Study- Google Warehouse-Scale Computer

Unit-V: VECTOR, SIMD AND GPU ARCHITECTURES

Introduction-Vector Architecture – SIMD Extensions for Multimedia – Graphics Processing Units – Case Studies – GPGPU Computing – Detecting and Enhancing Loop Level Parallelism-Case Studies.

Text Books:

1. Darryl Gove, —Multicore Application Programming: For Windows, Linux, and Oracle Solaris, Pearson, 2011
2. David B. Kirk, Wen-mei W. Hwu, —Programming Massively Parallel Processors, Morgan Kauffman, 2010

References:

Reference Books

1. David E. Culler, Jaswinder Pal Singh, "Parallel computing architecture : A hardware/software approach" , Morgan Kaufmann Elsevier Publishers, 1999
2. Kai Hwang and Zhi.Wei Xu, —Scalable Parallel Computing, Tata McGraw Hill, NewDelhi, 2003.

Journals:

1. IEEE Computer Architecture Letters
2. International Journal of Parallel Processing

Video Reference:

1. http://acl.digimat.in/nptel/courses/video/106102229/L27.html

NPTEL Courses:

1. Multi-Core Computer Architecture

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4. Course Outcomes

CO. No.	Course Outcome
P23VL524.1	Compare different advanced processor architectures, and understand their impact on performance and efficiency.
P23VL524.2	Design and optimize memory hierarchies, including cache systems and virtual memory, and apply techniques to address memory consistency and coherence in multi-core systems.
P23VL524.3	Utilize various parallel processing models and programming frameworks to develop and optimize parallel algorithms.
P23VL524.4	Analyze and design interconnection networks, including network topologies and communication protocols, to improve data transfer and overall system performance.
P23VL524.5	Investigate emerging technologies such as heterogeneous computing and quantum computing, and evaluate their potential impact on future computer architecture and parallel processing.

Semester IV

Sl.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
PRACTICALS								
1	P23VL602	Project Work Phase II	PW	32	0	0	32	16
		TOTAL		**32**	**0**	**0**	**32**	**16**

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OPEN ELECTIVES (OE)

Sl. No	Course Code	Subject	Course Category	L	T	P	C
1	P23OE501	Business Analytics	OE	3	0	0	3
2	P23OE502	Industrial Safety	OE	3	0	0	3
3	P23OE503	Operations Research	OE	3	0	0	3
4	P23OE507	Artificial Intelligence	OE	3	0	0	3
5	P23OE508	Machine Learning	OE	3	0	0	3

P23OE501	BUSINESS ANALYTICS	L	T	P	C
		3	0	0	3

1. Course Description:

In today's data-driven world, the ability to analyze and interpret data is crucial for effective decision-making in business. This course provides a comprehensive introduction to business analytics, focusing on the tools and techniques used to transform raw data into actionable insights. Students will explore key concepts such as data visualization, predictive analytics, and statistical analysis. The curriculum enables students to analyze real-world datasets and develop analytical models.

2. Course Objectives:

1. To develop the ability to collect, clean, and prepare data for analysis, ensuring accuracy and relevance in business contexts.
2. To apply descriptive and predictive analytics methods to identify trends, make forecasts, and support data-driven decision-making.
3. To create effective visual representations of data that clearly communicate insights and facilitate stakeholder understanding.
4. To gain hands-on experience with industry-standard analytics tools, enabling practical application of analytical techniques in real-world scenarios.
5. To understand how to integrate analytics into business strategies, enhancing organizational performance and decision-making processes.

3. Syllabus:

Unit-I: OVERVIEW OF BUSINESS ANALYTICS

Introduction; Drivers for Business Analytics; Applications of Business Analytics: Marketing and Sales, Human Resource, Healthcare, Product Design, Service Design, Customer Service and Support; Skills Required for a Business Analyst; Framework for Business Analytics Life Cycle for Business Analytics Process.

Unit-II: ESSENTIALS OF BUSINESS ANALYTICS

Descriptive Statistics; Using Data; Types of Data; Data Distribution Metrics: Frequency, Mean, Median, Mode, Range, Variance, Standard Deviation, Percentile, Quartile, z-Score, Covariance, Correlation; Data Visualization: Tables, Charts, Line Charts, Bar and Column Chart, Bubble Chart, Heat Map; Data Dashboards.

Unit-III: MODELING UNCERTAINTY AND STATISTICAL INFERENCE

Modeling Uncertainty: Events and Probabilities; Conditional Probability; Random Variables; Discrete Probability Distributions; Continuous Probability Distribution; Statistical Inference: Data Sampling; Selecting a Sample; Point Estimation; Sampling Distributions; Interval Estimation; Hypothesis Testing.

Unit-IV: ANALYTICS USING HADOOP AND MAPREDUCE FRAMEWORK

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Introducing Hadoop; RDBMS versus Hadoop; Hadoop Overview; HDFS (Hadoop Distributed File System); Processing Data with Hadoop; Introduction to MapReduce; Features of MapReduce; Algorithms Using Map-Reduce: Matrix-Vector Multiplication, Relational Algebra Operations, Grouping and Aggregation; Extensions to MapReduce.

Unit-V: OTHER DATA ANALYTICAL FRAMEWORKS

Overview of Application development Languages for Hadoop; Pig Latin; Hive; Hive Query Language (HQL); Introduction to Pentaho, JAQL; Introduction to Apache: Sqoop, Drill and Spark, Cloudera Impala; Introduction to NoSQL Databases; Hbase and MongoDB.

References:

Reference Books:

1. Vignesh Prajapati, "Big Data Analytics with R and Hadoop", Packt Publishing, 2013.
2. Anand Rajaraman, Jeffrey David Ullman, "Mining of Massive Datasets", Cambridge University Press, 2012.
3. Jeffrey D. Camm, James J. Cochran, Michael J. Fry, Jeffrey W. Ohlmann, David R. Anderson, "Essentials of Business Analytics", Cengage Learning, second Edition, 2016
4. U. Dinesh Kumar, "Business Analytics: The Science of Data-Driven Decision Making", Wiley, 2017.
5. A. Ohri, "R for Business Analytics", Springer, 2012
6. Umesh R Hodeghatta, UmeshaNayak, "Business Analytics Using R – A Practical Approach", Apress, 2017
7. Rui Miguel Forte, "Mastering Predictive Analytics with R", Packt Publication, 2015.

Video References:

1. https://www.youtube.com/watch?v=diaZdX1s5L4
2. https://www.youtube.com/watch?v=3kMSsb9MFQo

Web References:

1. https://www.tutorialspoint.com/business_analysis/index.htm
2. https://www.simplilearn.com/tutorials/business-analysis-tutorial

MOOC/SWAYAM/NPTEL Courses:

1. https://onlinecourses.nptel.ac.in/noc24_cs65/preview
2. https://www.coursera.org/specializations/business-analytics
3. https://www.udemy.com/courses/business/analytics-and-intelligence/

4. **Course Outcomes:**

After successful completion of the course, the student should be able to:

CO. No.	Course Outcome
P230E501.1	Identify the real-world business problems and model with analytical solutions.
P230E501.2	Solve analytical problem with relevant mathematics background knowledge
P230E501.3	Convert any real-world decision-making problem to hypothesis and apply suitable statistical testing
P230E501.4	Use open-source frameworks for modelling and storing data.
P230E501.5	Apply suitable visualization technique using R for visualizing voluminous data

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P23OE502	INDUSTRIAL SAFETY	L	T	P	C
		3	0	0	3

1. Course Description:

The Industrial Safety course provides a comprehensive overview of safety practices and regulations essential for maintaining a safe working environment in industrial settings. Students will learn to identify hazards, assess risks, and implement effective safety management systems. The curriculum covers key topics such as personal protective equipment (PPE), emergency preparedness, ergonomics, and the development of a safety culture within organizations.

2. Course Objectives:

1. To develop the ability to identify and assess potential hazards in industrial environments, utilizing effective risk assessment techniques.
2. To understand key safety regulations and standards that govern workplace safety and ensure compliance within industrial settings.
3. To design and implement safety management systems that promote a culture of safety and reduce workplace incidents.
4. To create and evaluate emergency response plans to effectively manage workplace emergencies and ensure employee safety.
5. To foster an organizational culture that encourages employee engagement and responsibility in maintaining a safe working environment.

3. Syllabus:

Unit-I: INTRODUCTION

Evolution of modern safety concepts; Fire prevention; Mechanical hazards; Boilers, Pressure vessels, Electrical Exposure.

Unit-II: CHEMICAL HAZARDS

Chemical exposure; Toxic materials; Ionizing Radiation and Non-ionizing Radiation; Industrial Hygiene; Industrial Toxicology.

Unit-III: ENVIRONMENTAL CONTROL

Industrial Health Hazards; Environmental Control; Industrial Noise; Noise measuring instruments, Control of Noise, Vibration; Personal Protection.

Unit-IV: HAZARD ANALYSIS

System Safety Analysis; Techniques; Fault Tree Analysis (FTA), Failure Modes and Effects Analysis (FMEA), HAZOP analysis and Risk Assessment.

Unit-V: SAFETY REGULATIONS

Explosions; Disaster management; catastrophe control, hazard control, Safety education and training; Factories Act, Safety regulations Product safety; case studies.

References:

Reference Books:

1. John V.Grimaldi, "Safety Management", AITB S Publishers, 2003.
2. Safety Manual, "EDEL Engineering Consultancy", 2000.
3. David L.Goetsch, "Occupational Safety and Health for Technologists", 5th Edition, Engineers and Managers, Pearson Education Ltd., 2005

Video References:

1. https://www.youtube.com/watch?v=jFDWlKayrTc&list=PLbRMhDVUMngdXebaRB59KdKwstzuAovua

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2. https://www.youtube.com/watch?v=RXtF_vQRebM

Web References:

1. https://safetytalker.com/safety-talks/general-industry-safety-rules/
2. https://www.tutorialspoint.com/workplace_safety/index.htm

MOOC/SWAYAM/NPTEL Courses:

1. https://onlinecourses.nptel.ac.in/noc19_me40/preview

https://www.coursera.org/specializations/chemical-hazards-and-process-safety

4. **Course Outcomes:**

After successful completion of the course, the student should be able to:

CO. No.	Course Outcome
P230E502.1	Get exposed to safety concepts and industry hazards
P230E502.2	Understand the chemical hazards
P230E502.3	Analyse the noise pollution using instruments
P230E502.4	Analyse the hazards using different techniques
P230E502.5	Apply the regulations for safety and control of hazards

P23OE503	OPERATIONS RESEARCH	L	T	P	C
		3	0	0	3

1. Course Description:

The Operations Research course provides an in-depth exploration of quantitative methods and analytical techniques used to optimize decision-making in complex systems. Students will learn to formulate and solve mathematical models related to resource allocation, scheduling, inventory management, and logistics. The curriculum covers key topics such as queuing theory, and decision analysis, integrating both theoretical concepts and practical applications.

2. Course Objectives:

1. To develop the ability to formulate real-world problems into mathematical models for analysis and optimization.
2. To apply various optimization methods, including linear programming and integer programming, to solve complex decision-making problems.
3. To utilize simulation techniques to analyze and improve system performance in scenarios with uncertainty.
4. To implement decision analysis tools and techniques to evaluate options and make informed choices in operations settings.
5. To gain hands-on experience in applying operations research methods to real-world case studies, enhancing problem-solving skills in diverse industries.

3. Syllabus:

Unit-I: OPERATIONS RESEARCH

The phase of an operation research study; Linear programming; Graphical method; Simplex algorithm; Duality formulation; Sensitivity analysis.

Unit-II: TRANSPORTATION MODELS AND NETWORK MODELS

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Transportation Assignment Models; Traveling Salesman Problem; Networks models; Shortest route; Minimal spanning tree; Maximum flow models; Project network; CPM and PERT networks; Critical path scheduling; Sequencing models.
Unit-III: INVENTORY MODELS
Inventory models; Economic order quantity models; Quantity discount models; Stochastic inventory models; Multi product models; Inventory control models in practice.
Unit-IV: QUEUING MODELS
Queueing models; Queueing systems and structures; Notation parameter; Single server and multi-server models; Poisson input; Exponential service; Constant rate service; Infinite population; Simulation.
Unit-V: DECISION MODELS
Decision models; Game theory; Two-person zero sum games; Graphical solution; Algebraic solution; Linear Programming solution; Replacement models; Models based on service life; Economic life; Single / Multi variability search technique; Dynamic Programming; Simple Problem.
References:
Reference Books: 1. Hillier and Libeberman, "Operations Research", Holden Day, 2005 2. Taha H.A., "Operations Research", Sixth Edition, Prentice Hall of India, 2003. 3. Bazara M.J., Jarvis and Sherali H., "Linear Programming and Network Flows", John Wiley, 2009. 4. Budnick F.S., "Principles of Operations Research for Management", Richard D Irwin, 1990. 5. Philip D.T. and Ravindran A., "Operations Research", John Wiley, 1992. 6. Shennoy G.V. and Srivastava U.K., "Operation Research for Management", Wiley Eastern, 1994. 7. Tulsian and Pasdey V., "Quantitative Techniques", Pearson Asia, 2002. **Video References:** 1. https://www.youtube.com/watch?v=KIKZyHTDR5Q&list=PLIY8eNdw5tW_UuFLy_vUP2pXNIHls2Pwd 2. https://www.youtube.com/watch?v=rDDmPvSVAII&list=PLEjRWorvdxL6ZDh5HbigDyuwgeW2WW0zs **Web References:** 1. https://mdu.ac.in/UpFiles/UpPdfFiles/2021/Jun/4_06-11-2021_16-06-34_OPERATIONS%20RESEARCH%20TECHNIQUES(20MAT22C5).pdf 2. http://ndl.ethernet.edu.et/bitstream/123456789/90288/6/Operations%20research%20handout.pdf **MOOC/SWAYAM/NPTEL Courses:** 1. https://onlinecourses.nptel.ac.in/noc22_ma48/preview 2. https://www.coursera.org/search?query=operations+research&language=English

4. **Course Outcomes:**

After successful completion of the course, the student should be able to:

CO. No.	Course Outcome
P230E503.1	Understand basics of operation research and optimization problems
P230E503.2	Apply transportation and network models
P230E503.3	Understand inventory control models
P230E503.4	Analyze the queueing systems and models
P230E503.5	Apply decision models for optimization problems

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P23OE507	ARTIFICIAL INTELLIGENCE	L	T	P	C
		3	0	0	3

1. Course Description:

This course offers a comprehensive exploration of the foundational principles and core concepts in Artificial Intelligence (AI). Beginning with an introduction to the history and applications of AI, the course progressively delves into intelligent agents, problem-solving, search algorithms, and extends to encompass knowledge representation and planning. Machine learning is a branch of artificial intelligence that enables systems to learn from data and improve their performance over time without being explicitly programmed. Students will gain a solid understanding of various machine learning algorithms, their theoretical underpinnings, and how to apply them both artificial intelligence and machine learning to real-world problems.

2. Course Objectives:

1. To study the structure of agents and the nature of environments
2. To learn the search algorithms of AI in different environments
3. To Learn and apply adversarial search techniques to solve problems in dynamic environments.
4. To understand the basic concepts of machine learning.
5. To understand and build supervised and unsupervised learning models.

3. Syllabus:

Unit-I: INTELLIGENT AGENTS

Introduction to artificial intelligence; Intelligent agents: agents & environment, concept of rationality, nature of environments, structure of agents.

Case Study: Autonomous Delivery Robots which interact with their surroundings and navigate through dynamic environments to deliver packages.

Unit-II: PROBLEM SOLVING AGENTS

Uninformed search strategies, Heuristic search strategies, heuristic functions; Local search and optimization problems, local search in continuous space, search with nondeterministic actions, search in partially observable environments, online search agents and unknown environments.

Case Study: Autonomous vehicle Navigation in Unknown Environments

Unit-III: GAME PLAYING AND CSP

Adversarial search: Games, optimal decisions in games, alpha - beta pruning, stochastic games, partially observable games; Constraint satisfaction problems; constraint propagation, backtracking search for CSP, local search for CSP, structure of CSP Case Study: Artificial intelligence system plays chess to make optimal moves in a partially observable and dynamic environment.

Unit-IV: SUPERVISED LEARNING

Machine Learning; Types of Machine Learning: Supervised Learning, Unsupervised Learning; Basic Concepts in Machine Learning ; Machine Learning Process; Weight Space; Testing Machine Learning Algorithms; A Brief Review of Probability Theory : Turning Data into Probabilities , The Bias-Variance Trade off. Linear Models for Regression; Linear Basis Function Models; The Bias-Variance Decomposition; Bayesian Linear Regression; Common Regression Algorithms: Simple Linear Regression, Multiple Linear Regression; Linear Models for Classification: Common Classification Algorithms: k-Nearest Neighbours, Decision Trees, Random Forest model, Support Vector Machines.

Unit-V: UNSUPERVISED LEARNING

Mixture Models and EM; K-Means Clustering; Dirichlet Process Mixture Models; Spectral Clustering; Hierarchical Clustering; The Curse of Dimensionality; Dimensionality Reduction: Principal Component Analysis; Latent Variable Models(LVM): Latent Dirichlet Allocation (LDA). Reinforcement Learning, Representation Learning – Neural Networks – Active Learning – Ensemble Learning – Bootstrap Aggregation – Boosting – Gradient Boosting Machines.

Text Books:

1. Stuart Russel and Peter Norvig, "Artificial Intelligence: A Modern Approach", Fourth Edition, Pearson Education, 2020.

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2. Ethem Alpaydin, "Introduction to Machine Learning", MIT Press, Fourth Edition, 2020.
3. Tom Mitchell, "Machine Learning", McGraw-Hill, 2017.

References:

Reference Books:

1. Deepak Khemani, "A First Course in Artificial Intelligence", McGraw Hill Education, New Delhi, 2017
2. Christopher Bishop, "Pattern Recognition and Machine Learning", Springer, 2006.
3. Kevin P. Murphy, "Machine Learning: A Probabilistic Perspective", MIT Press, 2012.

Video References:

1. https://www.youtube.com/watch?v=JxgmHe2NyeY
2. https://www.youtube.com/watch?v=z18nw4adsx4

Web References:

1. https://alex.smola.org/drafts/thebook.pdf
2. https://www.cin.ufpe.br/~cavmj/Machine%20-0Learning%20%20Tom%20Mitchell.pdf

MOOC/SWAYAM/NPTEL Courses:

1. Introduction to Machine learning- MIT OpenCourseWare
2. Essential Mathematics for Artificial Intelligence on edX

4. **Course Outcomes:**

After successful completion of the course, the student should be able to:

CO. No.	Course Outcome
P230E507.1	Implement a study of agents' structures and diverse environments in AI.
P230E507.2	Apply various AI search algorithms for different environmental scenarios using the knowledge and skills acquired.
P230E507.3	Implement a comprehensive study of adversarial search techniques and resolving constraint satisfaction problems in AI.
P230E507.4	Apply logical and probabilistic inference mechanisms to improve decision-making in AI systems.
P230E507.5	Analyze knowledge representation techniques and planning algorithms vital for Artificial Intelligence

P23OE508	MACHINE LEARNING	L	T	P	C
		3	0	0	3

1. Course Description:

This course provides an in-depth introduction to the fundamental concepts and techniques of machine learning, a field at the intersection of computer science and statistics that focuses on the development of algorithms capable of learning from data. Students will gain a comprehensive understanding of the principles and applications of machine learning, along with hands-on experience in implementing and evaluating machine learning models.

2. Course Objectives:

1. To explain the different types of Machine learning techniques and mathematical concepts
2. To use natural language processing technique using large language models
3. To apply the different machine learning tools to solve the real time problems
4. To make decisions using reinforcement learning and Markov Decision process.

3. Syllabus

Unit-I: INTRODUCTION

Review of Linear Algebra for Machine Learning. Introduction and motivation for machine learning; Types of Machine Learning: Supervised Learning, Unsupervised Learning and Reinforcement learning. Statistical Decision theory: Classification and Regression, Bias and Variance. Case Study: Stock Price Prediction

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Unit-II: CLASSIFICATION AND REGRESSION
Linear Regression, Multivariate Regression, Subset Selection, Shrinkage methods, Principal Components Regression, Partial Least Squares. Ridge and LASSO Regression. Logistic Regression. Linear Discriminant Analysis. Decision Tree, K Nearest Neighbor, Separating hyperplane – Perceptron learning Support Vector Machines and kernels. Artificial Neural Networks: Back propagation Algorithm, Maximum Likelihood estimate. Case Study: House Price Prediction using Linear Regression and spam email classification using support vector machine algorithm.
Unit-III: EVALUATION MEASURES AND ENSEMBLE TECHNIQUES
Evaluation Measures: Bootstrapping and cross validation ROC Curve, Minimum Description length and exploratory analysis. Ensemble Methods: Bagging, Committee machines, Stacking, Boosting, Gradient Boosting, Random Forest Case Study: Random Forest for Credit Scoring and Stacking for Image Classification
Unit-IV: BAYESIAN NETWORKS AND CLUSTERING
Naïve Bayes, Bayesian Networks, Undirected Graphical models, Hidden Markov models, Varaible Elimination, Belief Propagation; Partitional Clustering, Hierarchical Clustering, BIRCH and CURE algorithms, Density based Clustering, Spectral Clustering. Case Study: Analyze customer reviews to determine the sentiment (positive, negative, or neutral) associated with a product or service.
Unit-V: REINFORCEMENT LEARNING
Introduction to Reinforcement learning, Framework, Elements of Reinforcement learning, Markov Decision Process, Q – Learning in Python, Deep Q- learning. Case Study: Game Playing
Text Books:
1. Ethem Alpaydin, "Introduction to Machine Learning", Third Edition, Prentice Hall of India, 2015. 2. Tom Mitchell, "Machine Learning", McGraw-Hill, 2017. 3. Christopher Bishop, "Pattern Recognition and Machine Learning", Springer, 2006. 4. Kevin P. Murphy, "Machine Learning: A Probabilistic Perspective", MIT Press, 2012. 5. Stephen Marsland, "Machine Learning – An Algorithmic Perspective", Second Edition, CRC Press, 2014.
References:
Reference Books: 1. Fabio Nelli, "Python Data Analytics with Pandas, Numpy, and Matplotlib", Second Edition, Apress, 2018. Educational Publishers Inc., 2015. 2. Peter Flach, "Machine Learning: The Art and Science of Algorithms that Make Sense of Data", First Edition, Cambridge University Press, 2012. **Video References:** 1. https://www.ysoutube.com/c/3blue1brown 2. https://www.youtube.com/channel/UCfzlCWGWYyIQ0aLC5w48gBQ **Web References:** 1. https://www.youtube.com/channel/UCWN3xxRkmTPmbKwht9FuE5A 2. Machine Learning by Andrew Ng on Coursera **MOOC/SWAYAM/NPTEL Courses:** 1. Introduction to Deep Learning - MIT OpenCourseWare 2. Essential Mathematics for Artificial Intelligence on edX

4. Course Outcomes:

After successful completion of the course, the student should be able to:

CO. No.	Course Outcome
P23OE508.1	Apply the mathematical concepts of machinelearning to solve the real-time problems.
P23OE508.2	Apply the different types of machine learningand graphical modelling for data

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	analysis andvisualization.
P23OE508.3	Implement boosting algorithms using appropriate libraries and tune hyper parametersfor optimal performance.
P23OE508.4	Interpret and communicate the results obtainedfrom Bayesian network analysis and clusteringalgorithms in the context of specific applications.
P23OE508.5	Examine the Markov Decision Process and Reinforcement learning algorithms in simulatedenvironment.

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